

N3T035MP120D 1200 V 35 mΩ Silicon Carbide MOSFET

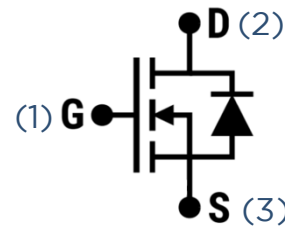
V_{DS}	I_D	$R_{DS(on)}$	Package
1200 V	76 A	35 mΩ	TO-247-3

Features

- State-of-the-art SiC MOSFET technology
- Reliable gate oxide process
- 100% avalanche tested
- Low input capacitance
- Low internal gate resistance
- Low body diode forward voltage drop

Benefits

- Higher system efficiency
- Reduced cooling requirements
- Increased power density
- Increased system switching frequency
- Enhanced system reliability
- Reduced total harmonic distortion



(1) (2) (3)

Applications

- Motor drives
- Solar PV inverters
- EV onboard chargers
- Server power supplies
- Energy storage systems
- EV fast charging stations
- Solid-state power controllers
- Uninterruptible power supplies

Maximum Ratings

Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit	Note
Drain-Source Voltage	$V_{(BR)DSS}$	$T_C = 25\text{ °C}$	1200	-	-	V	
Gate-Source Voltage	$V_{GS(max)}$		-10	-	25	V	
	$V_{GS,op}$	Recommended Operation	-	-5/+20	-		
Continuous Drain Current	I_D	$V_{GS} = 20\text{ V}, T_C = 25\text{ °C}$	-	-	76	A	Fig. 13
		$V_{GS} = 20\text{ V}, T_C = 100\text{ °C}$	-	-	54		
Pulsed Drain Current	$I_{D(pulse)}$	$T_C = 25\text{ °C}$ t_p limited by $T_{j(max)}$	-	-	160	A	Fig. 12
Power Dissipation	P_{tot}	$T_C = 25\text{ °C}$	-	-	319	W	Fig. 14
Avalanche Energy, Single Pulse	E_{AS}	$L = 26\text{ mH}, I_{AS} = 5.5\text{ A}$	-	393	-	mJ	
Operating and Storage Temperature	T_J, T_{stg}		-55	-	175	°C	

Thermal and Package Characteristics

Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit	Note
Thermal Resistance, Junction to Case	$R_{th(JC)}$		-	0.38	0.47	°C/W	Fig. 11
Thermal Resistance, Junction to Ambient	$R_{th(JA)}$		-	-	40	°C/W	
Weight	W_T		-	6.34	-	g	
Solder Temperature	T_L	JEDEC J-STD-020	-	-	225	°C	
Mounting Torque	T_M	M3 or 6-32 screw	-	0.9	-	Nm	

Electrical Characteristics ($T_c = 25\text{ °C}$ unless otherwise specified)

STATIC CHARACTERISTICS

Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit	Note
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	$V_{GS} = 0\text{ V}$, $I_D = 100\text{ QA}$	1200	-	-	V	
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = 1200\text{ V}$, $V_{GS} = 0\text{ V}$	-	1	100	QA	
Gate Threshold Voltage	$V_{GS(th)}$	$V_{GS} = V_{DS}$, $I_D = 25\text{ mA}$	1.8	2.4	3	V	
Gate-Source Leakage Current	I_{GSS}	$V_{GS} = -10 / +25\text{ V}$, $V_{DS} = 0\text{ V}$	-	-	±100	nA	
Transconductance	g_{fs}	$V_{DS} = 20\text{ V}$, $I_D = 30\text{ A}$	-	17.3	-	S	Fig. 8
Drain-Source On-State Resistance	$R_{DS(on)}$	$V_{GS} = 20\text{ V}$, $I_D = 30\text{ A}$	-	30	45	mΩ	Fig. 4, 5, 6
		$V_{GS} = 20\text{ V}$, $I_D = 30\text{ A}$, $T_c = 175\text{ °C}$	-	55	-		
		$V_{GS} = 18\text{ V}$, $I_D = 30\text{ A}$	-	32	-		
		$V_{GS} = 18\text{ V}$, $I_D = 30\text{ A}$, $T_c = 175\text{ °C}$	-	56	-		

DYNAMIC CHARACTERISTICS

Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit	Note
Input Capacitance	C_{iss}	$V_{GS} = 0 \text{ V}, V_{DS} = 800 \text{ V}, V_{AC} = 25 \text{ mV}, f = 1 \text{ MHz}$	-	2204	-	pF	Fig. 10
Output Capacitance	C_{oss}		-	126	-		
Reverse Capacitance	C_{rss}		-	12	-		
Gate-Source Charge	Q_{GS}	$V_{DS} = 800 \text{ V}, V_{GS} = -5 / +20 \text{ V}, I_D = 30 \text{ A}$	-	24	-	nC	Fig. 15
Gate-Drain Charge	Q_{GD}		-	22	-		
Total Gate Charge	Q_G		-	126	-		
Internal Gate Resistance	$R_{G(int)}$	$V_{AC} = 25 \text{ mV}, f = 1 \text{ MHz}$	-	1.8	-	Ω	
Turn-On Switching Energy	E_{ON}	$V_{DD} = 800 \text{ V}, I_D = 30 \text{ A}, V_{GS} = -5 / +20 \text{ V}, R_{G(ext)} = 2 \text{ Ω}, L = 500 \text{ QH}$	-	578	-	QJ	Fig. 16 Fig. 17 Fig. 18
Turn-Off Switching Energy	E_{OFF}		-	331	-		
Total Switching Energy	E_{TOT}		-	909	-		
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = 800 \text{ V}, I_D = 30 \text{ A}, V_{GS} = -5 / +20 \text{ V}, R_{G(ext)} = 2 \text{ Ω}, L = 500 \text{ QH}$ Timing relative to V_{DS} Inductive Load	-	12	-	ns	Fig. 19
Rise Time	t_r		-	36	-		
Turn-Off Delay Time	$t_{d(off)}$		-	47	-		
Fall Time	t_f		-	14	-		

BODY DIODE CHARACTERISTICS

Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit	Note
Diode Forward Voltage	V_{SD}	$V_{GS} = -5 \text{ V}, I_{SD} = 30 \text{ A}$	-	4.3	-	V	Fig. 20
		$V_{GS} = -5 \text{ V}, I_{SD} = 30 \text{ A}, T_C = 175 \text{ °C}$	-	3.84	-	V	Fig. 21
Continuous Diode Forward Current	I_S	$V_{GS} = -5 \text{ V}$	-	61	-	A	
Reverse Recovery Time	t_{rr}	$V_R = 800 \text{ V}, I_{SD} = 30 \text{ A}, V_{GS} = -5 \text{ V}, di_F/dt = 1000 \text{ A/Qs}$	-	23	-	ns	
Reverse Recovery Charge	Q_{rr}		-	156	-	nC	
Peak Reverse Recovery Current	I_{RRM}		-	11.5	-	A	

Typical Performance

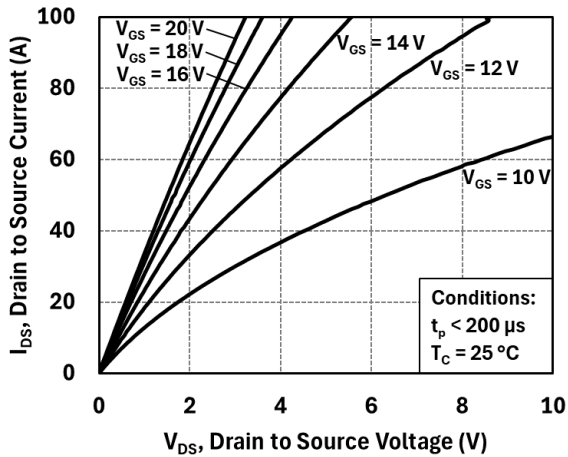


Figure 1: Output Characteristics at 25°C

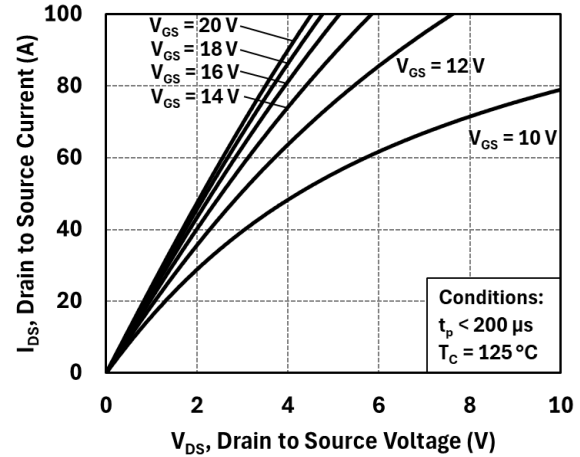


Figure 2: Output Characteristics at 125°C

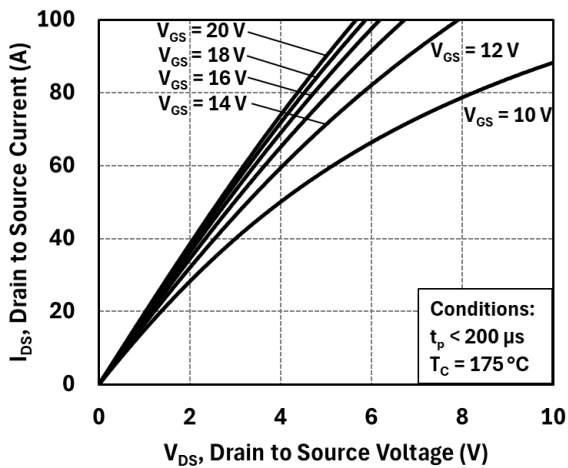


Figure 3: Output Characteristics at 175°C

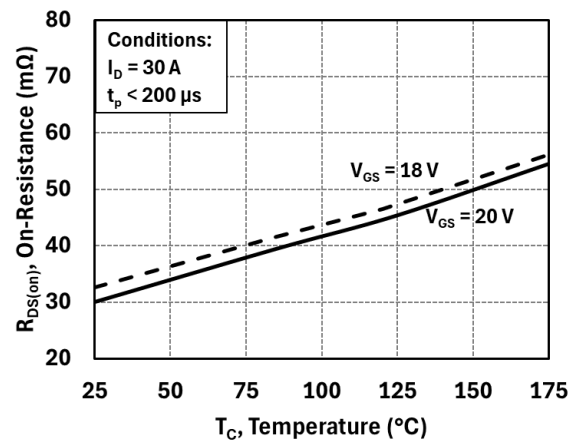


Figure 4: On-Resistance vs. Temperature

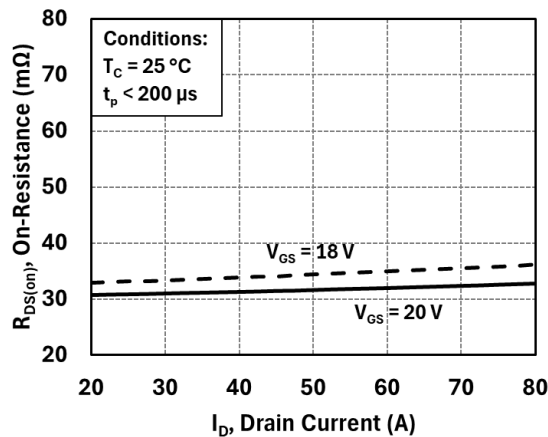


Figure 5: On-Resistance vs. Drain Current

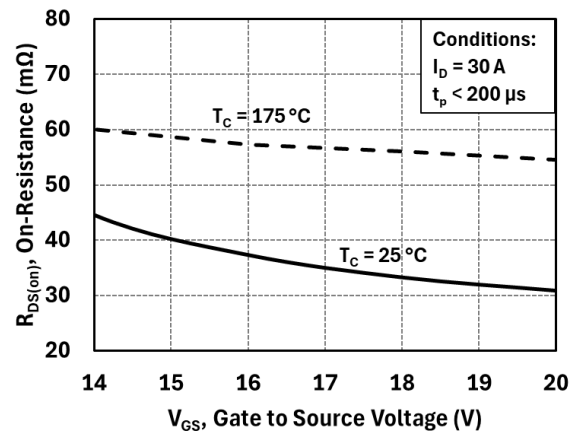


Figure 6: On-Resistance vs. Gate Voltage



Typical Performance

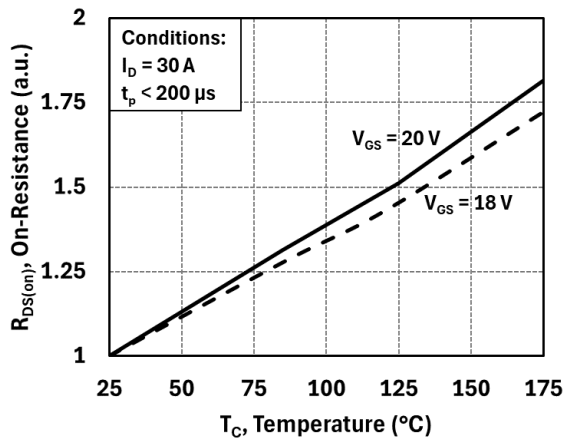


Figure 7: Normalized On-Resistance vs. Temperature

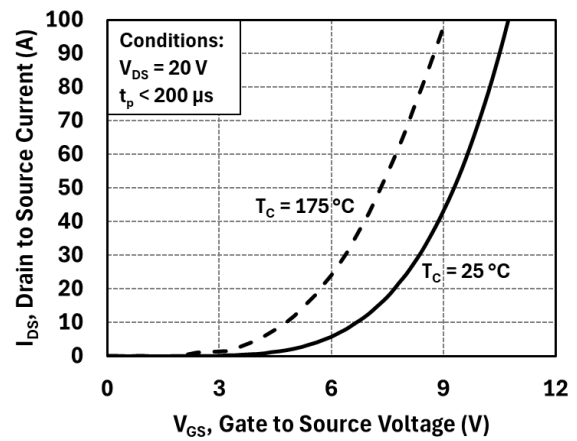


Figure 8: Transfer Characteristics

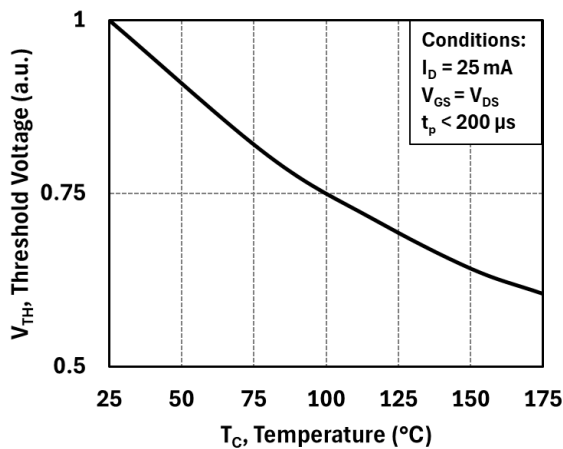


Figure 9: Threshold Voltage vs. Temperature

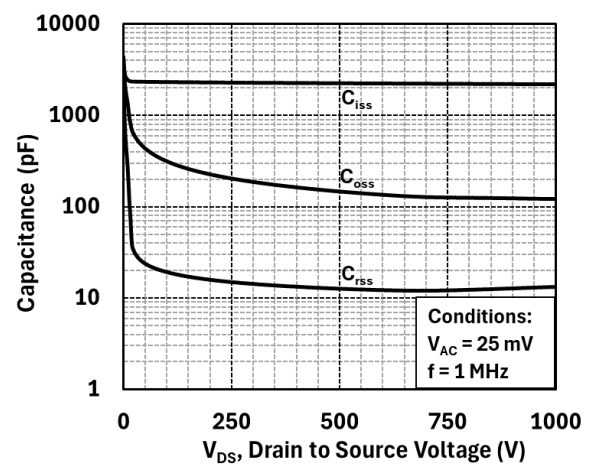


Figure 10: Capacitances vs. Drain-Source Voltage (0-1000 V)

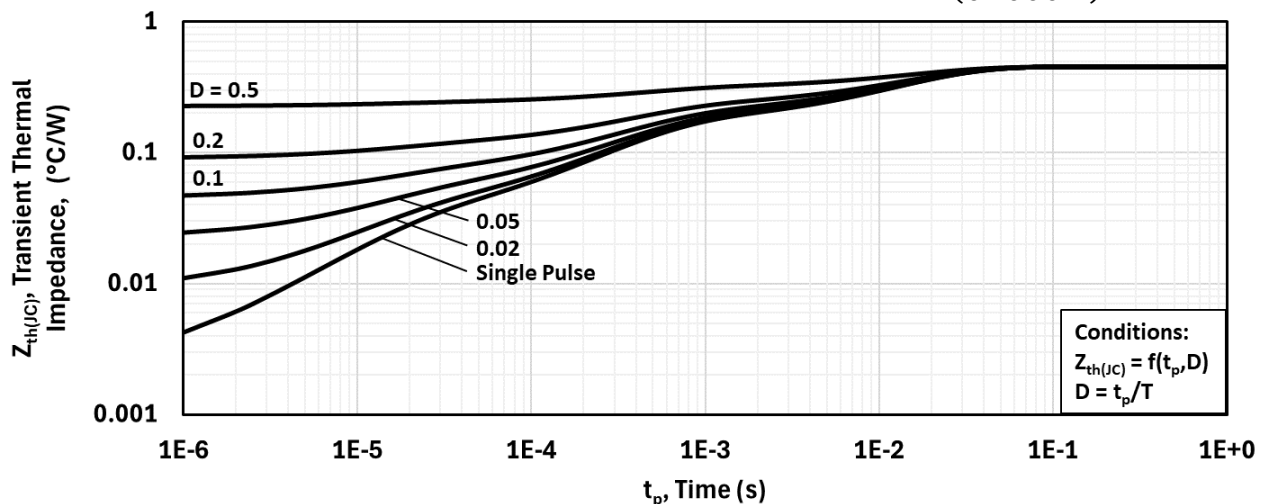


Figure 11: Transient Thermal Impedance





Typical Performance

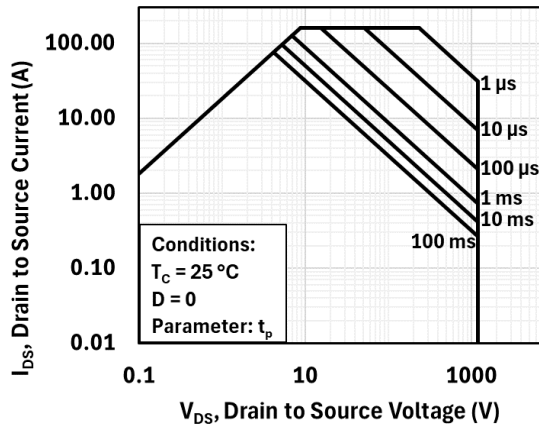


Figure 12: Safe Operating Area

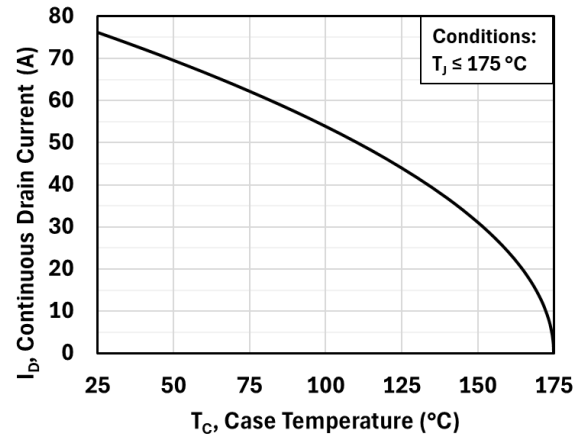


Figure 13: Current Derating Curve

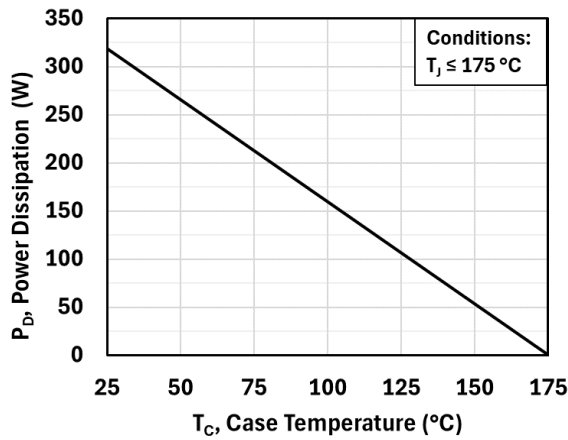


Figure 14: Power Derating Curve

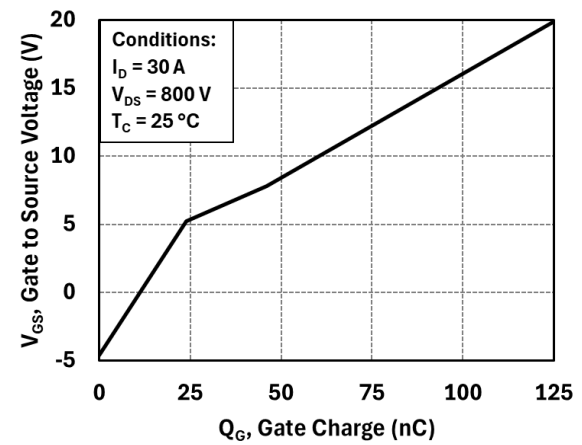


Figure 15: Gate Charge Characteristics

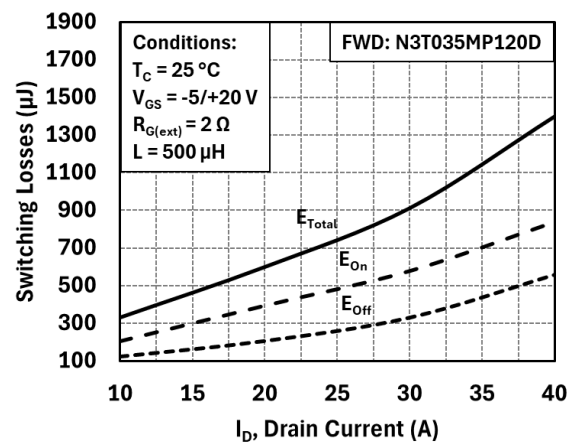


Figure 16: Inductive Switching Energy vs. Drain Current ($V_{DD} = 800\text{ V}$)

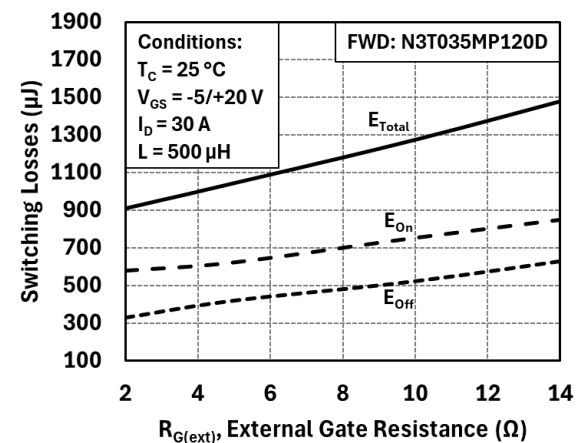


Figure 17: Inductive Switching Energy vs. $R_{G(ext)}$ ($V_{DD} = 800\text{ V}$)



Typical Performance

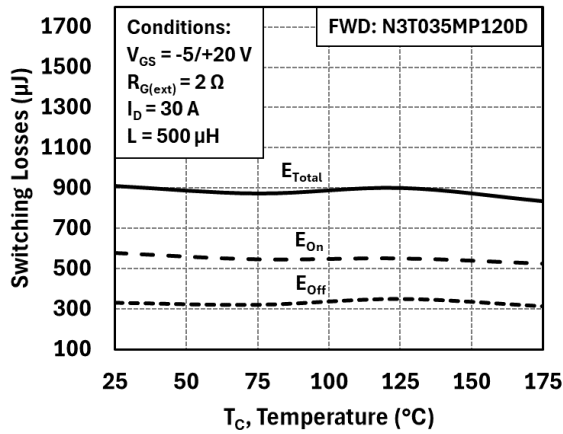


Figure 18: Inductive Switching Energy vs. Temperature ($V_{\text{DD}} = 800\text{ V}$)

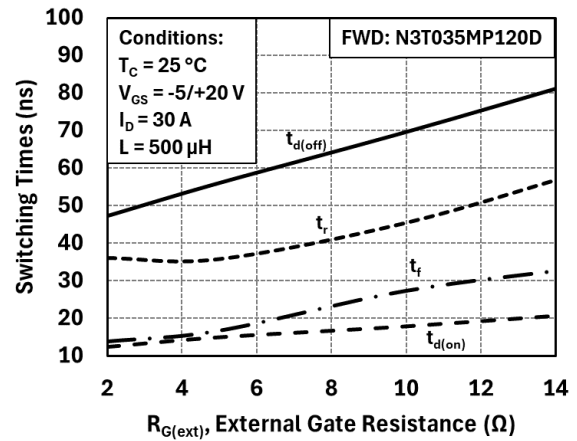


Figure 19: Switching Times vs. $R_{\text{G(ext)}}$ ($V_{\text{DD}} = 800\text{ V}$)

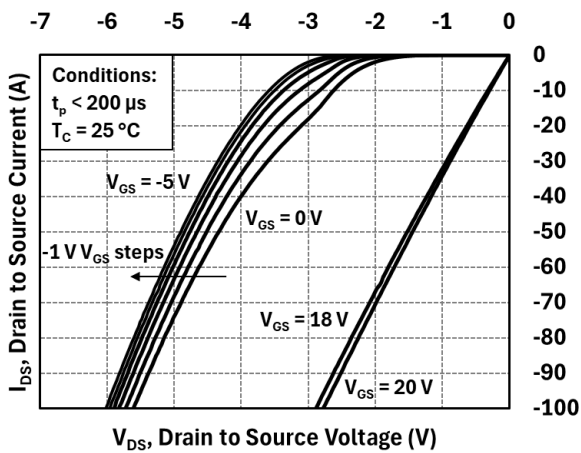


Figure 20: Body Diode Characteristics at 25 $^{\circ}\text{C}$

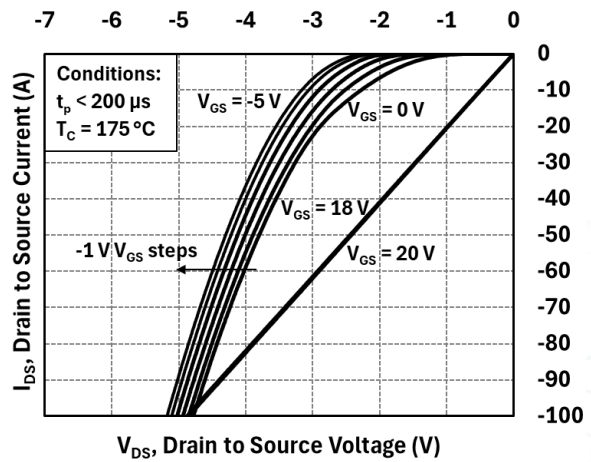


Figure 21: Body Diode Characteristics at 175 $^{\circ}\text{C}$

Dynamic Testing Circuit Schematics

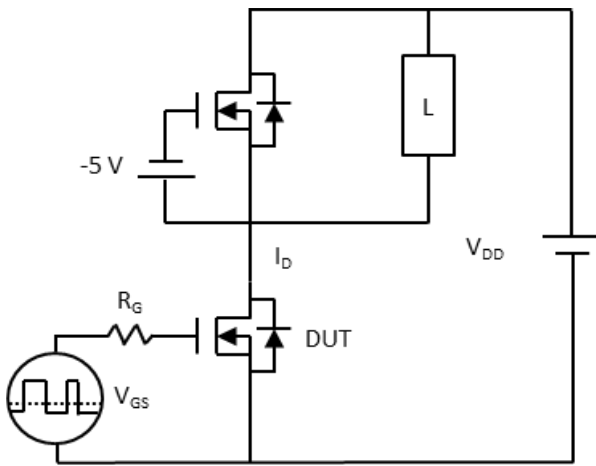


Figure 22: Inductive Load Switching Test Circuit

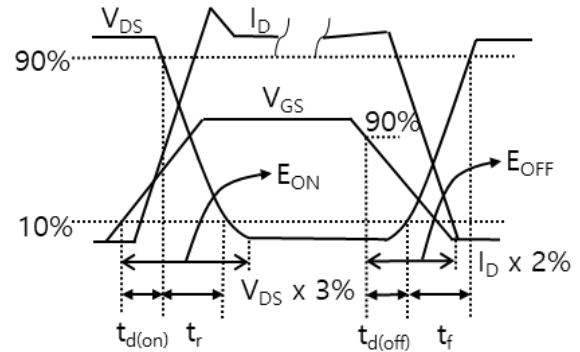


Figure 23: Inductive Load Switching Test Waveforms

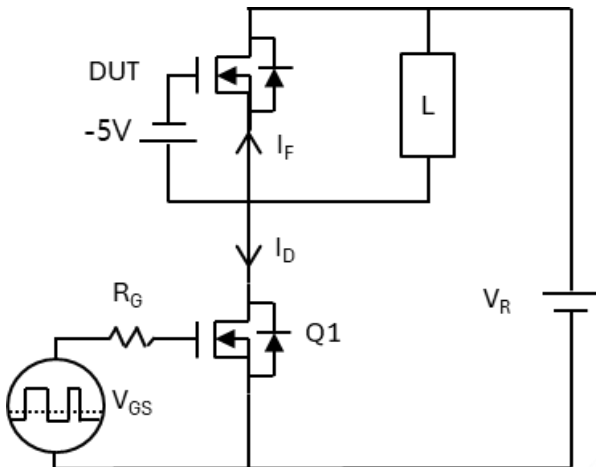


Figure 24: Reverse Recovery Test Circuit

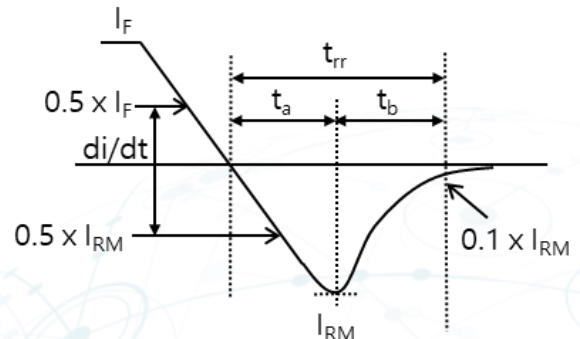


Figure 25: Body Diode Reverse Recovery Test Waveforms

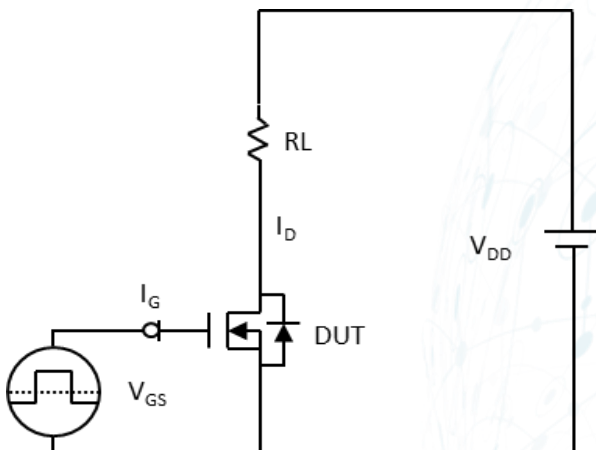


Figure 26: Gate Charge Test Circuit

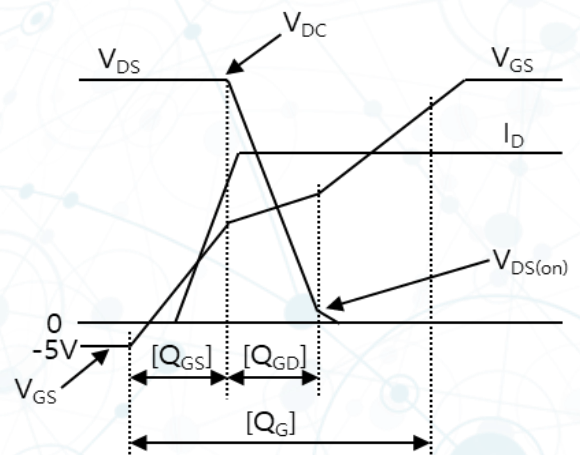
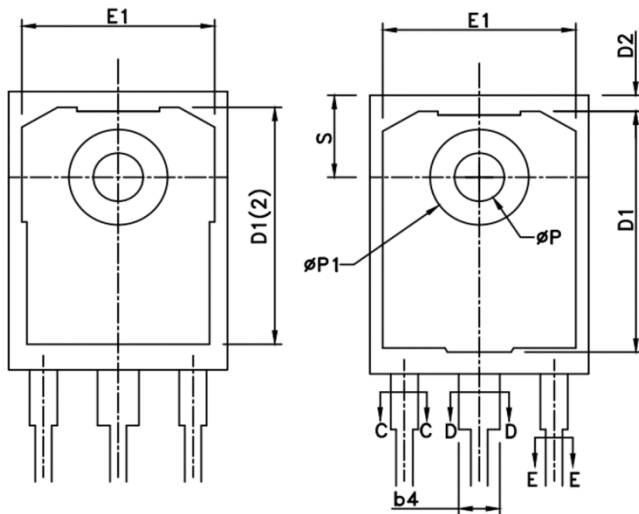
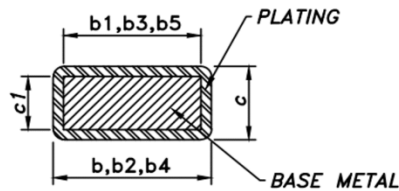
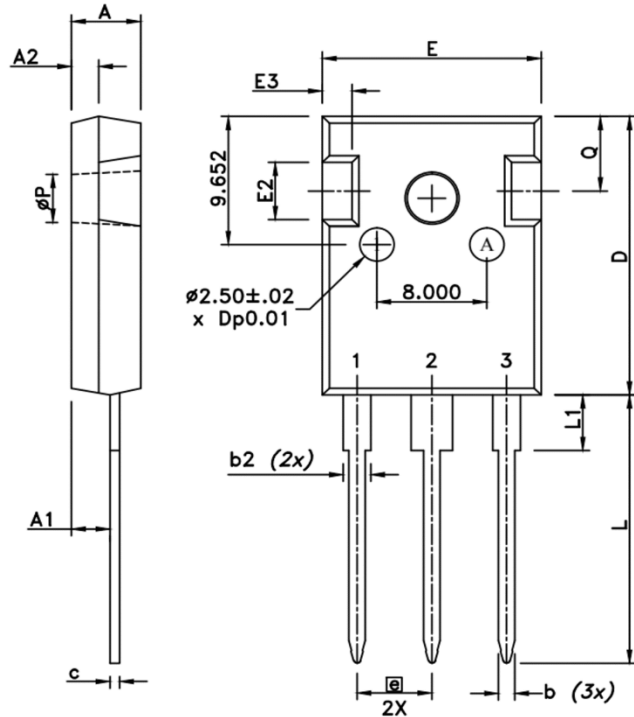


Figure 27: Gate Charge Test Waveforms

Package Dimensions



BACK SIDE (HEATSINK BASED ON LEADFRAME USED)


SECTION C-C, D-D, E-E
NOT TO SCALE


AREA	MIN	NOM	MAX
A	4.902	5.029	5.156
A1	2.253	2.380	2.507
A2	1.854	1.981	2.108
D	20.828	20.955	21.082
E	15.773	15.900	16.027
E2	4.191	4.318	4.445
E3	2.100	2.356	2.613
e	5.385	5.436	5.487
L	20.066	20.193	20.320
L1	3.937	4.191	4.445
ØP	3.556	3.607	3.658
Q	5.486	5.613	5.740
S	6.045	6.172	6.299
b	0.991	—	1.397
b1	0.991	1.199	1.346
b2	1.651	—	2.387
b3	1.651	1.999	2.336
b4	2.591	—	3.429
b5	2.591	3.000	3.378
c	0.381	0.635	0.889
c1	0.381	0.610	0.838
D1	17.187	17.314	17.441
D1(2)	16.881	17.008	17.135
D2	1.067	1.194	1.321
E1	13.894	14.021	14.148
ØP1	7.061	7.188	7.315

NOTES:

1. DIMENSIONS ARE IN MILLIMETERS
2. DIMENSION D & E DO NOT INCLUDE MOLD FLASH, MOLD FLASH SHALL NOT EXCEED 0.127 MM PER SIDE. THESE DIMENSIONS ARE MEASURED AT THE OUTERMOST EXTREME OF THE PLASTIC BODY.
3. ØP TO HAVE A MAXIMUM DRAFT ANGLE OF 1.5° TO THE TOP OF THE PART WITH A MAXIMUM HOLE DIAMETER OF 0.154".
4. ACTUAL DIMENSIONS OF E2 AND E3 ARE CLOSED TO MINIMUM SPECIFICATIONS.
5. *E3 IS NON-COMPLIANT WITH JEDEC.

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