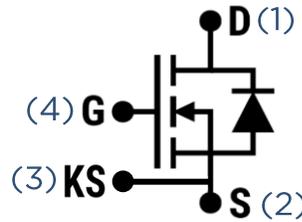


N3PT100MP170K

1700 V 100 mΩ Silicon Carbide MOSFET

V_{DS}	I_D	$R_{DS(on)}$	Package
1700 V	24 A	100 mΩ	TO-247-4



(1) (2) (3) (4)

Features

- State-of-the-art SiC MOSFET technology
- Reliable gate oxide process
- Ultra-low input capacitance
- Best-in-class figure-of-merits, [$R_{on} \cdot C_{iss}$] and [$R_{on} \cdot C_{rss}$]
- Stable switching characteristics up to 175 °C

Benefits

- Higher system efficiency
- Reduced cooling requirements
- Increased power density
- Increased system switching frequency
- Enhanced system reliability
- Reduced total harmonic distortion

Applications

- Rail/traction (~1.5 kV DC bus systems), including auxiliary circuits
- Renewable/wind/solar high voltage converters
- Industrial high-voltage drives
- Commercial EV/heavy-duty & DC fast chargers
- Defense/Aerospace/Maritime high voltage systems

Maximum Ratings

Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit	Note
Drain-Source Voltage	$V_{(BR)DSS}$	$T_C = 25\text{ °C}$	1700	-	-	V	
Gate-Source Voltage	$V_{GS(max)}$		-10	-	25	V	
	$V_{GS,op}$	Recommended Operation	-	-5/+20	-		
Continuous Drain Current	I_D	$V_{GS} = 20\text{ V}, T_C = 25\text{ °C}$	-	-	24	A	Fig. 13
		$V_{GS} = 20\text{ V}, T_C = 100\text{ °C}$	-	-	17		
Pulsed Drain Current	$I_{D(pulse)}$	$T_C = 25\text{ °C}$	-	-	80	A	Fig. 12
Power Dissipation	P_{tot}	$T_C = 25\text{ °C}$	-	-	136	W	Fig. 14
Operating and Storage Temperature	T_J, T_{stg}		-55	-	175	°C	

Thermal and Package Characteristics

Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit	Note
Thermal Resistance, Junction to Case	R_{thJC}		-	0.67	1.1	°C/W	Fig. 11
Thermal Resistance, Junction to Ambient	R_{thJA}		-	-	40	°C/W	
Weight	W_T		-	6.5	-	g	
Solder Temperature	T_L	JEDEC J-STD-020	-	-	225	°C	
Mounting Torque	T_M	M3 or 6-32 screw	-	0.9	-	Nm	

Electrical Characteristics ($T_c = 25\text{ °C}$ unless otherwise specified)

STATIC CHARACTERISTICS

Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit	Note
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	$V_{GS} = 0\text{ V}, I_D = 100\text{ }\mu\text{A}$	1700	-	-	V	
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = 0\text{ V}, V_{GS} = 0\text{ V}$	-	1	100	μA	
Gate Threshold Voltage	$V_{GS(th)}$	$V_{GS} = V_{DS}, I_D = 10\text{ mA}$	1.8	2.7	3.4	V	
Gate-Source Leakage Current	I_{GSS}	$V_{GS} = -10 / +25\text{ V}, V_{DS} = 0\text{ V}$	-	-	± 100	nA	
Transconductance	g_{fs}	$V_{DS} = 10\text{ V}, I_D = 15\text{ A}$	-	6.7	-	S	Fig. 8
Drain-Source On-State Resistance	$R_{DS(on)}$	$V_{GS} = 20\text{ V}, I_D = 15\text{ A}$	-	108	120	mΩ	Fig. 1
		$V_{GS} = 20\text{ V}, I_D = 15\text{ A}, T_C = 175\text{ °C}$	-	245	-	mΩ	Fig. 3
		$V_{GS} = 18\text{ V}, I_D = 15\text{ A}$	-	115	-	mΩ	Fig. 1
		$V_{GS} = 18\text{ V}, I_D = 15\text{ A}, T_C = 175\text{ °C}$	-	250	-	mΩ	Fig. 3

DYNAMIC CHARACTERISTICS

Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit	Note
Input Capacitance	C_{iss}	$V_{GS} = 0\text{ V}, V_{DS} = 1000\text{ V}, V_{AC} = 25\text{ mV}, f = 1\text{ MHz}$	-	1050	-	pF	Fig. 10
Output Capacitance	C_{oss}		-	38	-		
Reverse Capacitance	C_{rss}		-	2.7	-		
Gate-Source Charge	Q_{GS}	$V_{DS} = 1000\text{ V}, V_{GS} = -5 / +20\text{ V}, I_D = 15\text{ A}$	-	16	-	nC	Fig. 15
Gate-Drain Charge	Q_{GD}		-	13	-		
Total Gate Charge	Q_G		-	67	-		
Internal Gate Resistance	$R_{G(int)}$	$V_{AC} = 25\text{ mV}, f = 1\text{ MHz}$	-	3.1	-	Ω	
Turn-On Switching Energy	E_{ON}	$V_{DD} = 1200\text{ V}, I_D = 15\text{ A}, V_{GS} = -5 / +20\text{ V}, R_{G(ext)} = 5\text{ Ω}, L = 500\text{ μH}$	-	310	-	μJ	Fig. 16 Fig. 17 Fig. 18
Turn-Off Switching Energy	E_{OFF}		-	79	-		
Total Switching Energy	E_{TOT}		-	389	-		
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = 1200\text{ V}, I_D = 15\text{ A}, V_{GS} = -5 / +20\text{ V}, R_{G(ext)} = 5\text{ Ω}, L = 500\text{ μH}$ Timing relative to V_{DS} Inductive Load	-	11	-	ns	Fig. 19
Rise Time	t_r		-	16	-		
Turn-Off Delay Time	$t_{d(off)}$		-	24	-		
Fall Time	t_f		-	13	-		

BODY DIODE CHARACTERISTICS

Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit	Note
Diode Forward Voltage	V_{SD}	$V_{GS} = -5\text{ V}, I_{SD} = 15\text{ A}$	-	5.0	-	V	Fig. 20
		$V_{GS} = -5\text{ V}, I_{SD} = 15\text{ A}, T_J = 175\text{ °C}$	-	4.3	-	V	Fig. 21
Continuous Diode Forward Current	I_S	$V_{GS} = -5\text{ V}$	-	24	-	A	
Reverse Recovery Time	t_{rr}	$V_R = 1200\text{ V}, I_{SD} = 15\text{ A}, V_{GS} = -5\text{ V}, diF/dt = 2000\text{ A/μs}$	-	14	-	ns	
Reverse Recovery Charge	Q_{rr}		-	116	-	nC	
Peak Reverse Recovery Current	I_{RRM}		-	15.2	-	A	

Typical Performance

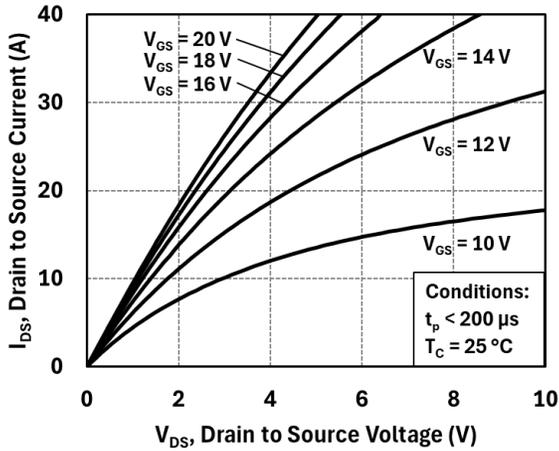


Figure 1: Output Characteristics at 25 °C

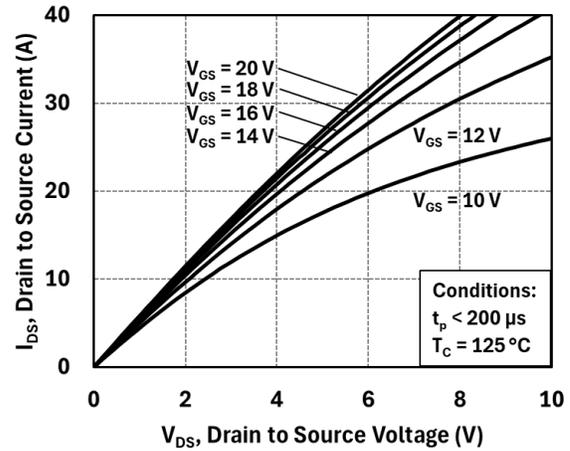


Figure 2: Output Characteristics at 125 °C

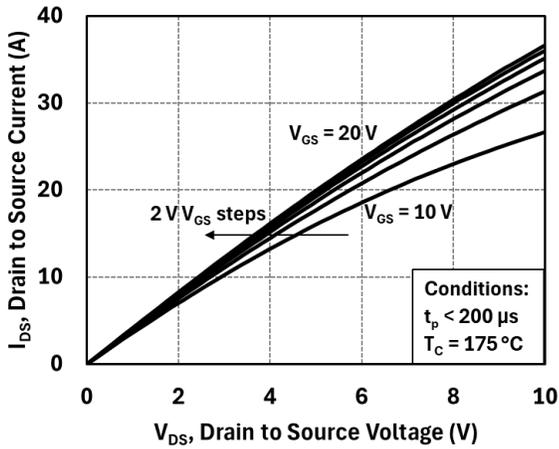


Figure 3: Output Characteristics at 175 °C

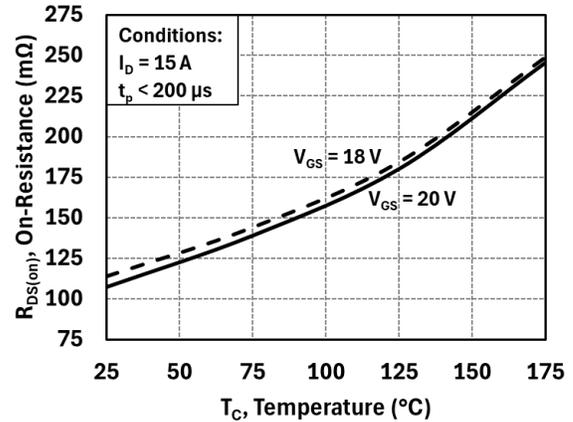


Figure 4: On-Resistance vs. Temperature

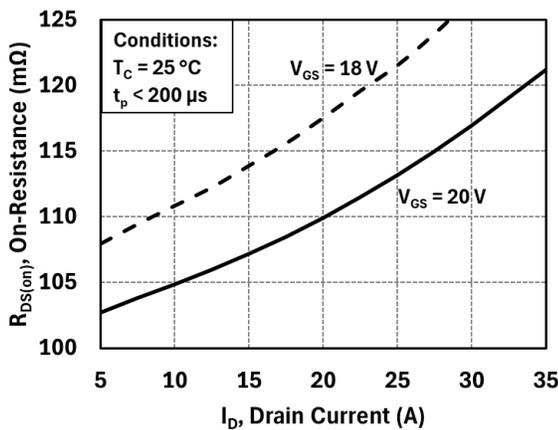


Figure 5: On-Resistance vs. Drain Current

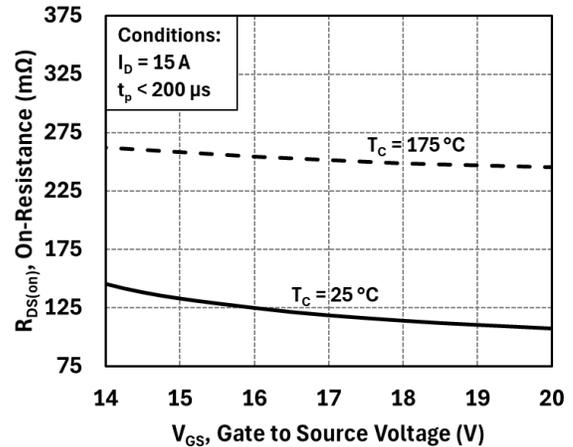


Figure 6: On-Resistance vs. Gate Voltage

Typical Performance

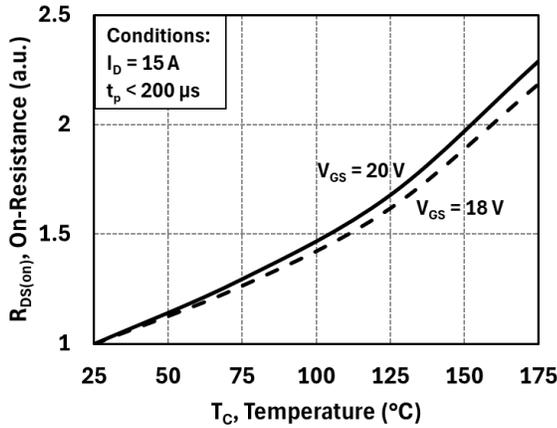


Figure 7: Normalized On-Resistance vs. Temperature

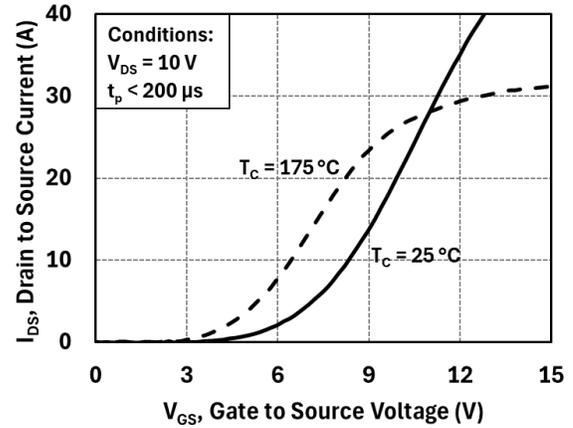


Figure 8: Transfer Characteristics

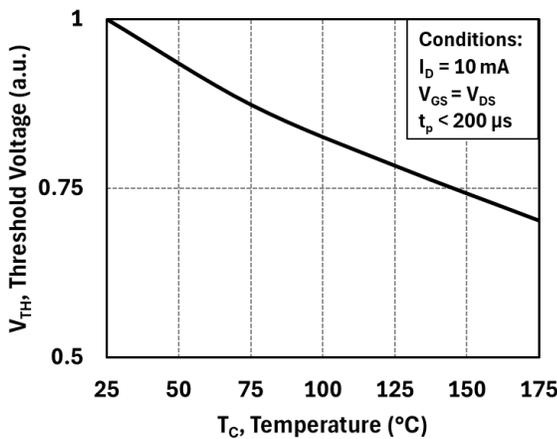


Figure 9: Threshold Voltage vs. Temperature

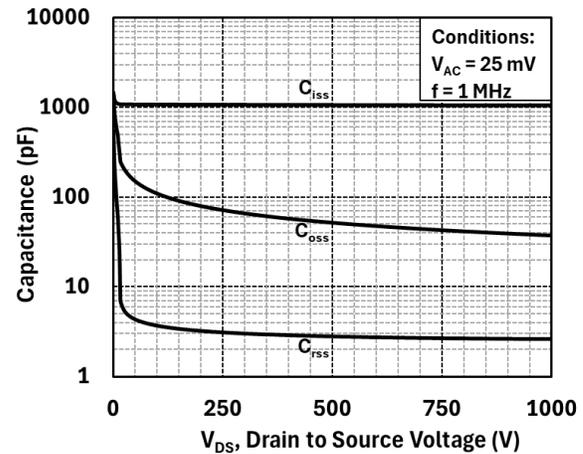


Figure 10: Capacitances vs. Drain-Source Voltage (0-1000 V)

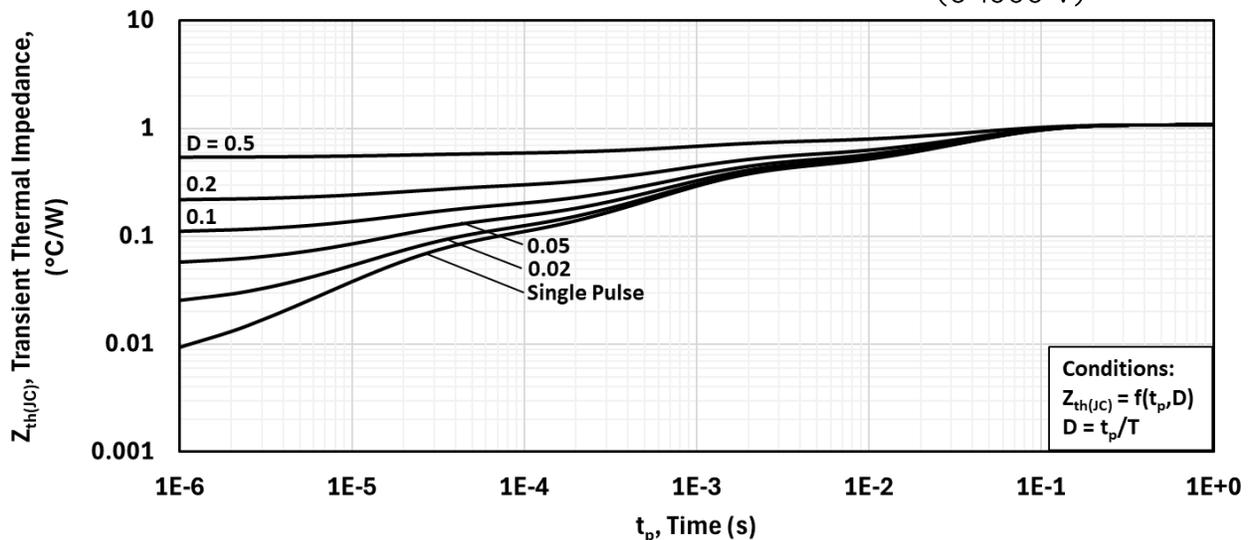


Figure 11: Transient Thermal Impedance

Typical Performance

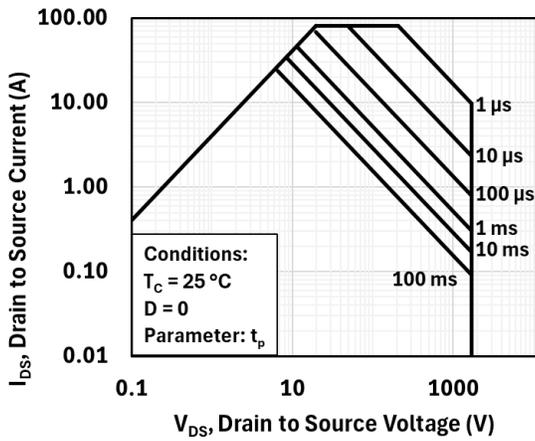


Figure 12: Safe Operating Area

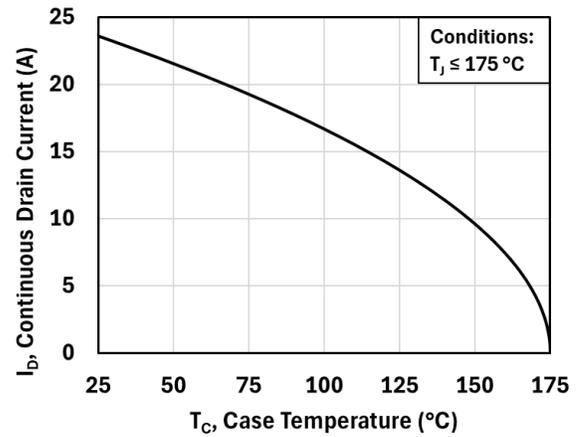


Figure 13: Current De-rating Curve

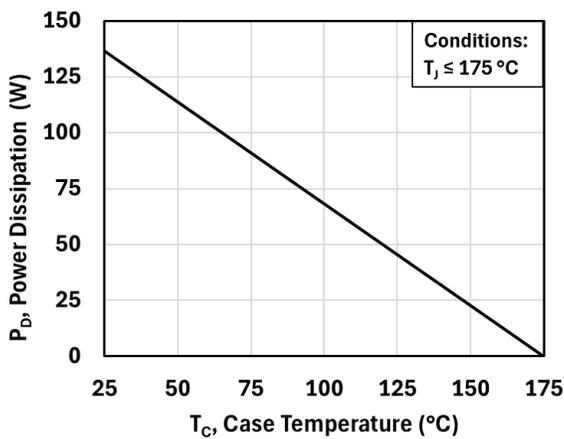


Figure 14: Power De-rating Curve

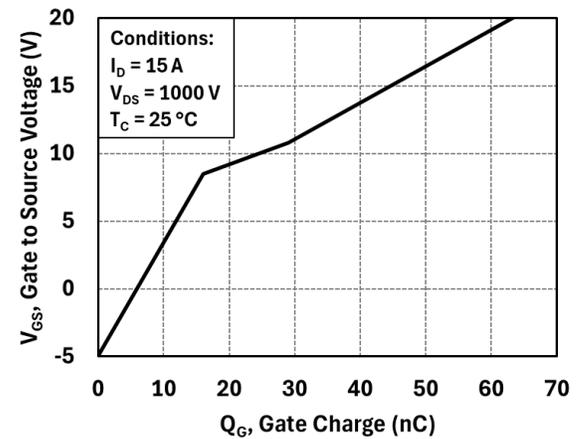


Figure 15: Gate Charge Characteristics

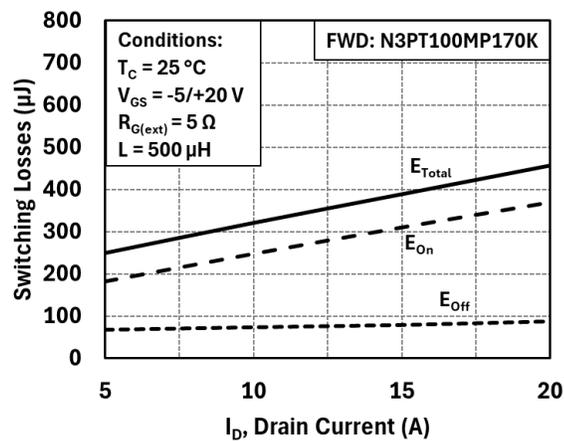


Figure 16: Inductive Switching Energy vs. Drain Current ($V_{DD} = 1200\text{ V}$)

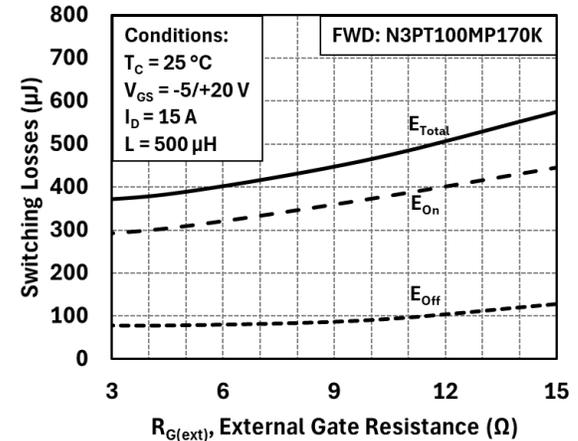


Figure 17: Inductive Switching Energy vs. $R_{G(ext)}$ ($V_{DD} = 1200\text{ V}$)

Typical Performance

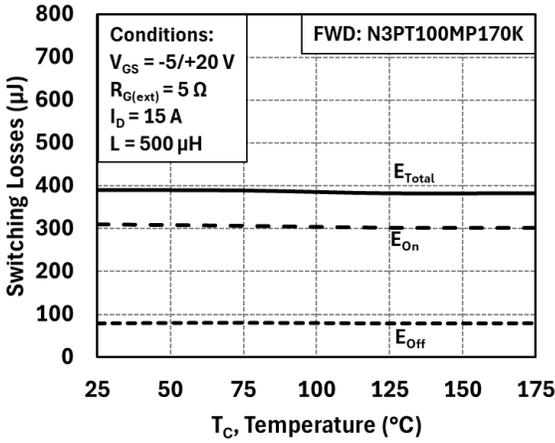


Figure 18: Inductive Switching Energy vs. Temperature (V_{DD} = 1200 V)

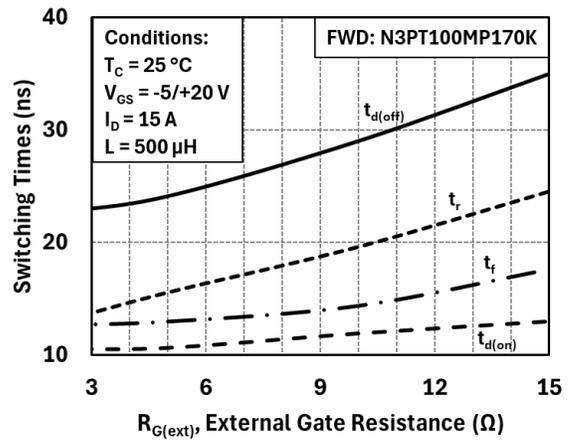


Figure 19: Switching Times vs. R_{G(ext)} (V_{DD} = 1200 V)

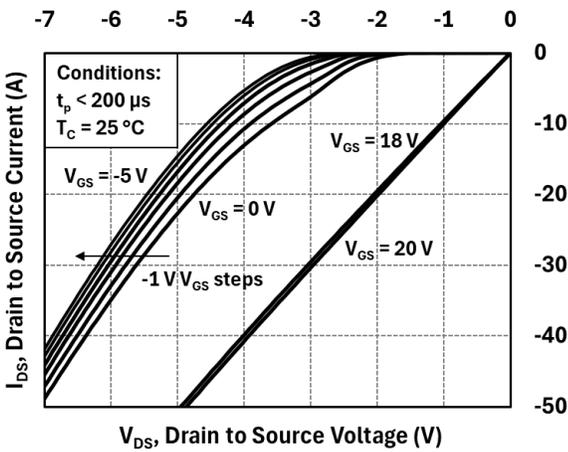


Figure 20: Body Diode Characteristics at 25 °C

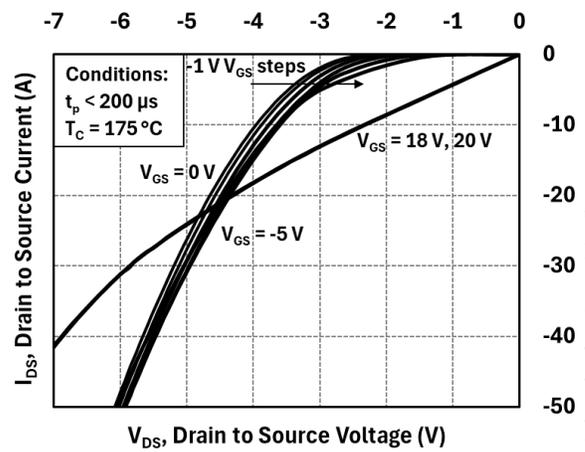


Figure 21: Body Diode Characteristics at 175 °C

Dynamic Testing Circuit Schematics

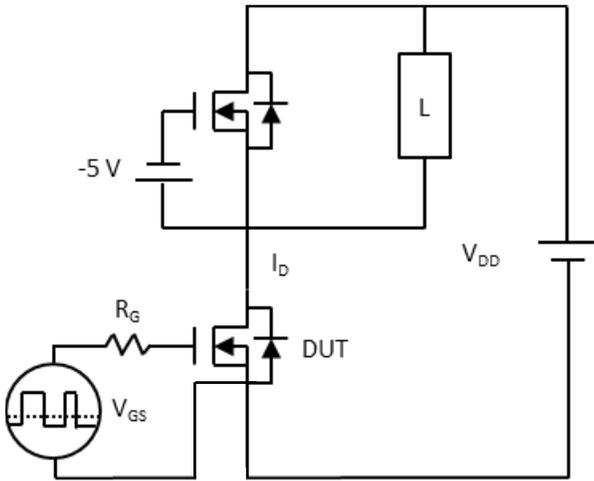


Figure 22: Inductive Load Switching Test Circuit

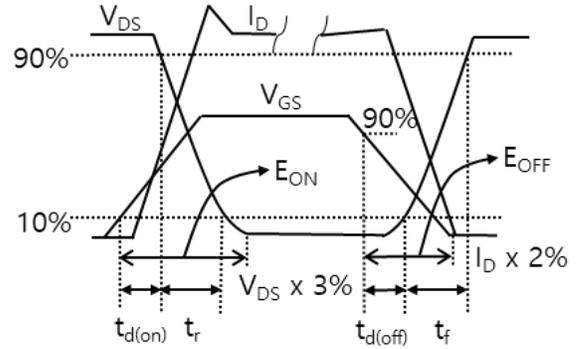


Figure 23: Inductive Load Switching Test Waveforms

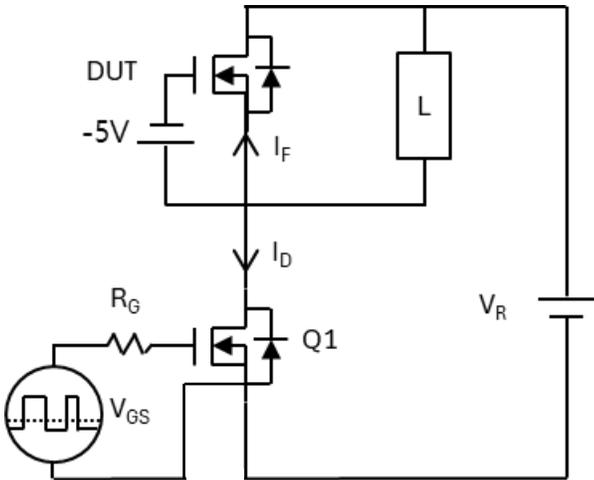


Figure 24: Reverse Recovery Test Circuit

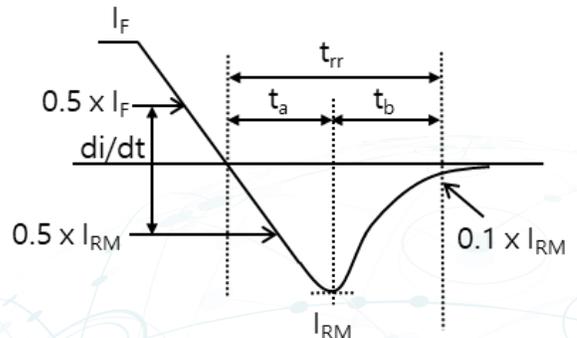


Figure 25: Body Diode Reverse Recovery Test Waveforms

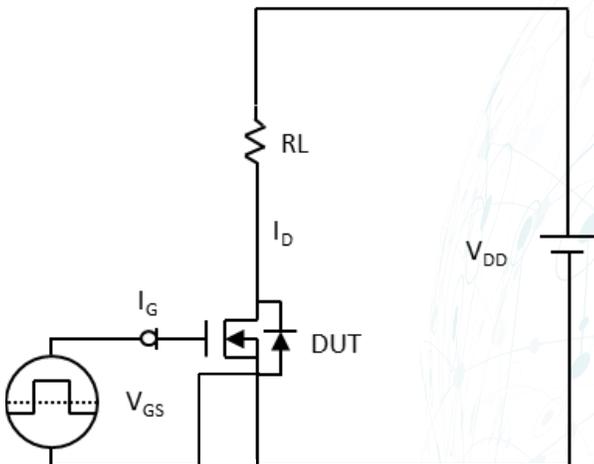


Figure 26: Gate Charge Test Circuit

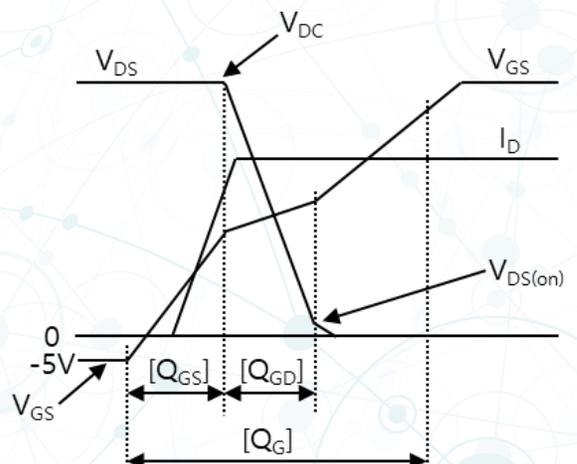
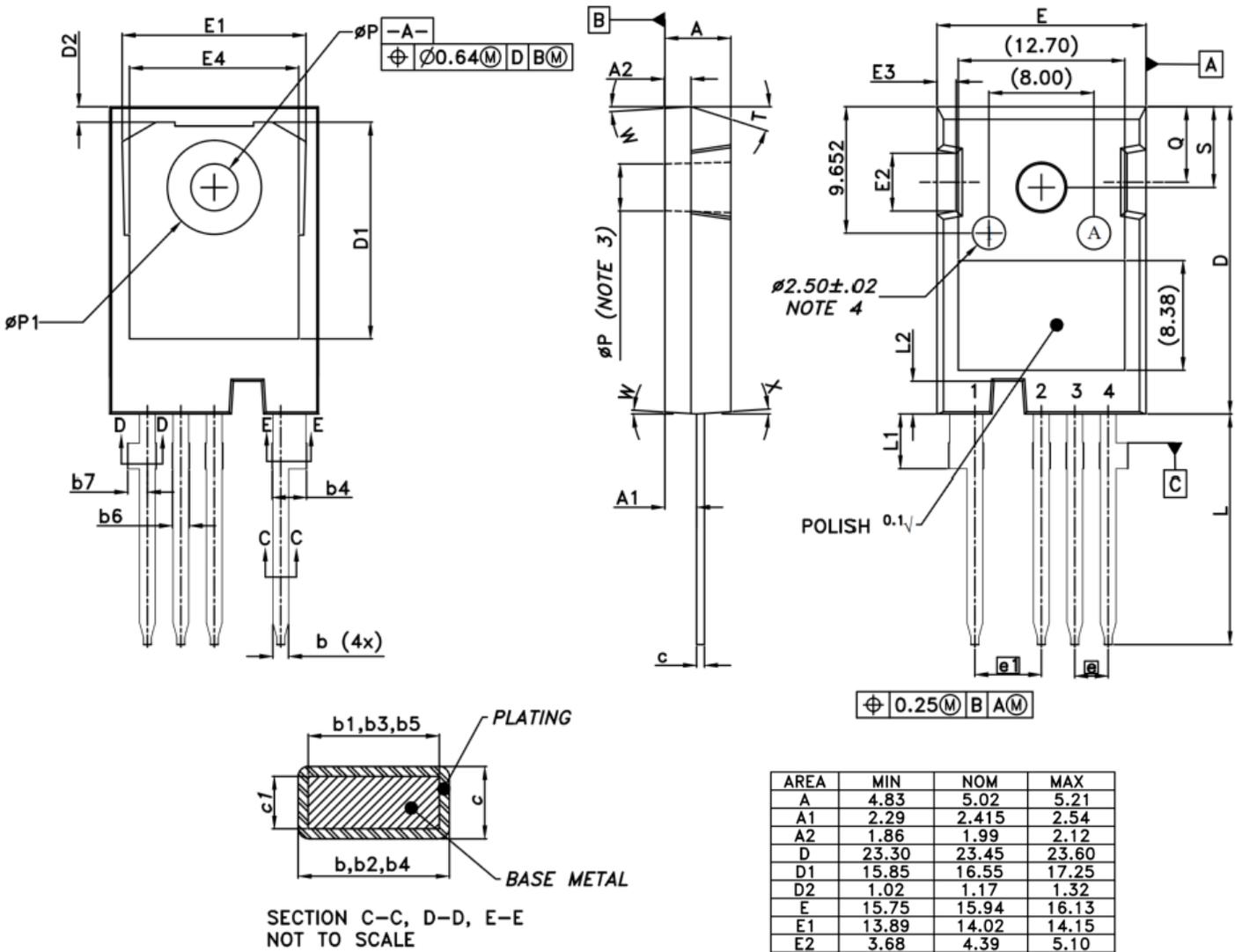


Figure 27: Gate Charge Test Waveforms

Package Dimensions



NOTES:

1. DIMENSIONS ARE IN MILLIMETERS
2. DIMENSION D & E DO NOT INCLUDE MOLD FLASH, MOLD FLASH SHALL NOT EXCEED 0.127 MM PER SIDE. THESE DIMENSIONS ARE MEASURED AT THE OUTERMOST EXTREME OF THE PLASTIC BODY.
3. øP TO HAVE A MAXIMUM DRAFT ANGLE OF 1.5° TO THE TOP OF THE PART WITH A MAXIMUM HOLE DIAMETER OF 3.65mm.
4. EJECTION MARK DEPTH 0.10^{+0.15}/_{0.08}

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