

N3PT065MP120K 1200 V 65 mΩ Silicon Carbide MOSFET

V_{DS}	I_D	$R_{DS(on)}$	Package
1200 V	40 A	65 mΩ	TO-247-4

Features

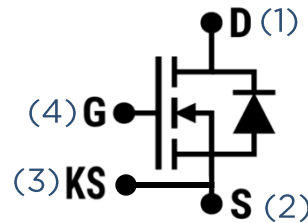
- State-of-the-art SiC MOSFET technology
- Reliable gate oxide process
- 100% avalanche tested
- Low input capacitance
- Best-in-class figure-of-merits, $[R_{on} \cdot C_{iss}]$ and $[R_{on} \cdot C_{rss}]$
- Stable switching characteristics up to 175 °C

Benefits

- Higher system efficiency
- Reduced cooling requirements
- Increased power density
- Increased system switching frequency
- Enhanced system reliability
- Reduced total harmonic distortion

Maximum Ratings

Parameter	Symbol	Test Conditions	Min.	Typ.	Max	Unit	Note
Drain-Source Voltage	$V_{(BR)DSS}$	$T_C = 25\text{ °C}$	1200	-	-	V	
Gate-Source Voltage	$V_{GS(max)}$		-10	-	25	V	
	$V_{GS,op}$	Recommended Operation	-	-5/+20	-		
Continuous Drain Current	I_D	$V_{GS} = 20\text{ V}, T_C = 25\text{ °C}$	-	-	40	A	Fig. 13
		$V_{GS} = 20\text{ V}, T_C = 100\text{ °C}$	-	-	28		
Pulsed Drain Current	$I_{D(pulse)}$	$T_C = 25\text{ °C}$	-	-	80	A	Fig. 12
Power Dissipation	P_{tot}	$T_C = 25\text{ °C}$	-	-	174	W	Fig. 14
Avalanche Energy, Single Pulse	E_{AS}	$L = 26\text{ mH}, I_{AS} = 3.5\text{ A}$	-	160		mJ	
Operating and Storage Temperature	T_J, T_{stg}		-55	-	175	°C	



Applications

- Motor drives
- Solar PV inverters
- EV onboard chargers
- Server power supplies
- Energy storage systems
- EV fast charging stations
- Solid-state power controllers
- Uninterruptible power supplies

Thermal and Package Characteristics

Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit	Note
Thermal Resistance, Junction to Case	R_{thJC}		-	0.71	0.86	°C/W	Fig. 11
Thermal Resistance, Junction to Ambient	R_{thJA}		-	-	40	°C/W	
Weight	W_T		-	6.12	-	g	
Solder Temperature	T_L	JEDEC J-STD-020	-	-	225	°C	
Mounting Torque	T_M	M3 or 6-32 screw	-	0.9	-	Nm	

Electrical Characteristics ($T_c = 25\text{ °C}$ unless otherwise specified)

STATIC CHARACTERISTICS

Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit	Note
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	$V_{GS} = 0\text{ V}$, $I_D = 100\text{ }\mu\text{A}$	1200	-	-	V	
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = 1200\text{ V}$, $V_{GS} = 0\text{ V}$	-	1	100	μA	
Gate Threshold Voltage	$V_{GS(th)}$	$V_{GS} = V_{DS}$, $I_D = 10\text{ mA}$	1.8	2.5	3	V	
Gate-Source Leakage Current	I_{GSS}	$V_{GS} = -10 / +25\text{ V}$, $V_{DS} = 0\text{ V}$	-	-	± 100	nA	
Transconductance	g_{fs}	$V_{DS} = 10\text{ V}$, $I_D = 20\text{ A}$	-	9.9	-	S	Fig. 8
Drain-Source On-State Resistance	$R_{DS(on)}$	$V_{GS} = 20\text{ V}$, $I_D = 20\text{ A}$	-	58	70	mΩ	Fig. 1
		$V_{GS} = 20\text{ V}$, $I_D = 20\text{ A}$, $T_C = 175\text{ °C}$	-	108	-	mΩ	Fig. 3
		$V_{GS} = 18\text{ V}$, $I_D = 20\text{ A}$	-	63	-	mΩ	Fig. 1
		$V_{GS} = 18\text{ V}$, $I_D = 20\text{ A}$, $T_C = 175\text{ °C}$	-	111	-	mΩ	Fig. 3

DYNAMIC CHARACTERISTICS

Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit	Note
Input Capacitance	C_{iss}	$V_{GS} = 0 \text{ V}, V_{DS} = 800 \text{ V}, V_{AC} = 25 \text{ mV}, f = 100 \text{ kHz}$	-	975	-	pF	Fig. 10
Output Capacitance	C_{oss}		-	57.6	-		
Reverse Capacitance	C_{rss}		-	3.8	-		
Gate-Source Charge	Q_{GS}	$V_{DS} = 800 \text{ V}, V_{GS} = -5 / +20 \text{ V}, I_D = 20 \text{ A}$	-	8	-	nC	Fig. 15
Gate-Drain Charge	Q_{GD}		-	11	-		
Total Gate Charge	Q_G		-	51	-		
Internal Gate Resistance	$R_{G(int)}$	$V_{AC} = 25 \text{ mV}, f = 1 \text{ MHz}$	-	2.9	-	Ω	
Turn-On Switching Energy	E_{ON}	$V_{DD} = 800 \text{ V}, I_D = 20 \text{ A}, V_{GS} = -5 / +20 \text{ V}, R_{G(ext)} = 5 \text{ } \Omega, L = 500 \text{ } \mu\text{H}$	-	280	-	μJ	Fig. 16 Fig. 17 Fig. 18
Turn-Off Switching Energy	E_{OFF}		-	41	-		
Total Switching Energy	E_{TOT}		-	321	-		
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = 800 \text{ V}, I_D = 20 \text{ A}, V_{GS} = -5 / +20 \text{ V}, R_{G(ext)} = 5 \text{ } \Omega, L = 500 \text{ } \mu\text{H}$ Timing relative to V_{DS} Inductive Load	-	13	-	ns	Fig. 19
Rise Time	t_r		-	14	-		
Turn-Off Delay Time	$t_{d(off)}$		-	29	-		
Fall Time	t_f		-	11	-		

BODY DIODE CHARACTERISTICS

Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit	Note
Diode Forward Voltage	V_{SD}	$V_{GS} = -5 \text{ V}, I_{SD} = 20 \text{ A}$	-	4.8	-	V	Fig. 20
		$V_{GS} = -5 \text{ V}, I_{SD} = 20 \text{ A}, T_J = 175 \text{ } ^\circ\text{C}$	-	4.3	-	V	Fig. 21
Continuous Diode Forward Current	I_S	$V_{GS} = -5 \text{ V}$	-	32	-	A	
Reverse Recovery Time	t_{rr}	$V_R = 800 \text{ V}, I_{SD} = 20 \text{ A}, V_{GS} = -5 \text{ V}, di_F/dt = 1000 \text{ A}/\mu\text{s}$	-	17	-	ns	
Reverse Recovery Charge	Q_{rr}		-	102	-	nC	
Peak Reverse Recovery Current	I_{RRM}		-	10	-	A	



Typical Performance

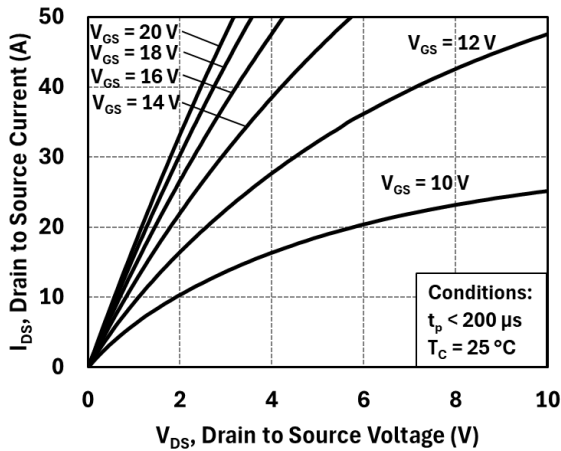


Figure 1: Output Characteristics at 25 °C

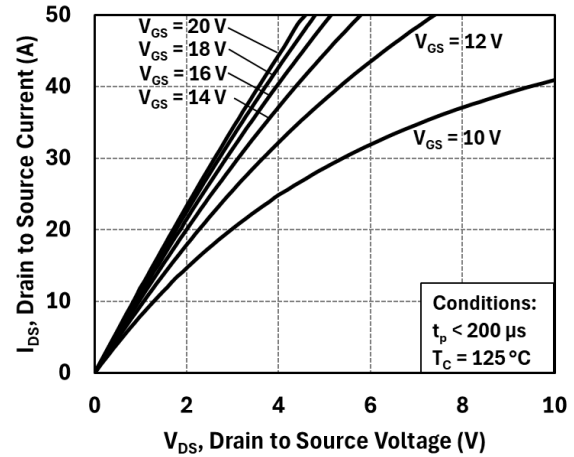


Figure 2: Output Characteristics at 125 °C

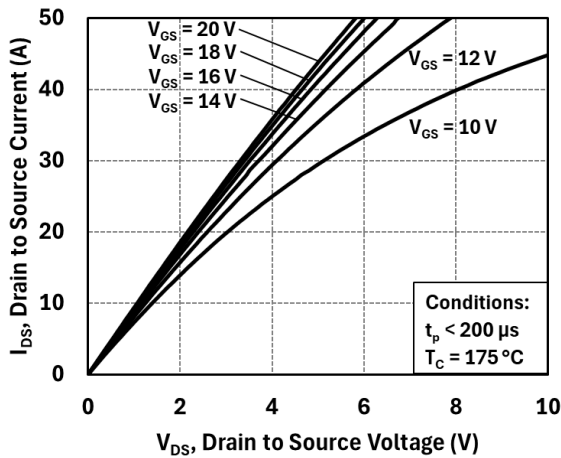


Figure 3: Output Characteristics at 175 °C

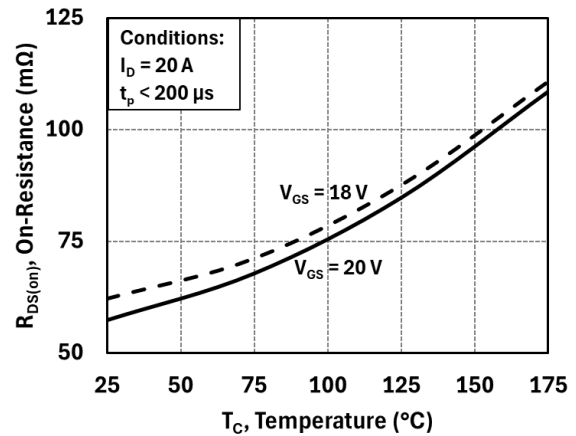


Figure 4: On-Resistance vs. Temperature

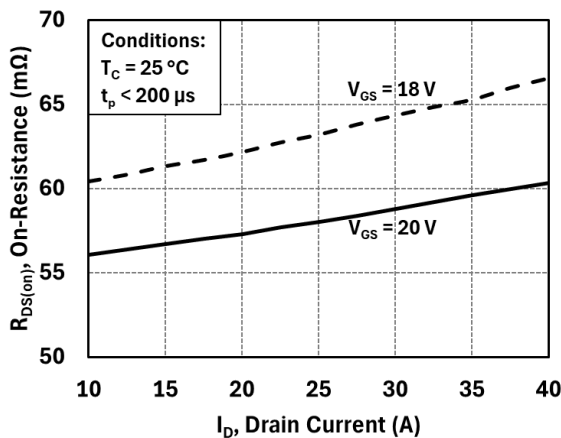


Figure 5: On-Resistance vs. Drain Current

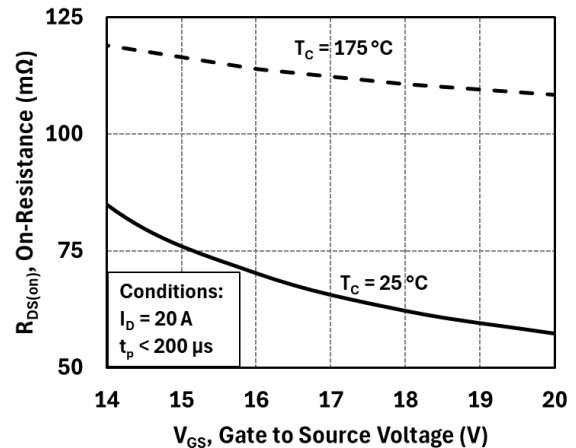


Figure 6: On-Resistance vs. Gate Voltage





Typical Performance

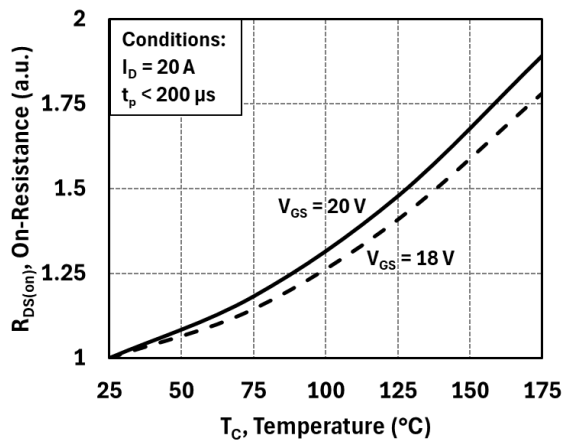


Figure 7: Normalized On-Resistance vs. Temperature

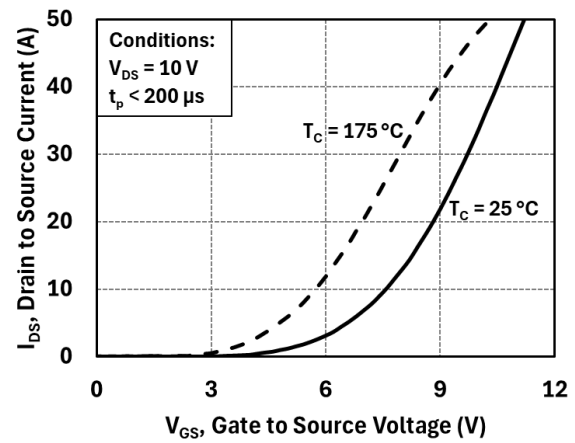


Figure 8: Transfer Characteristics

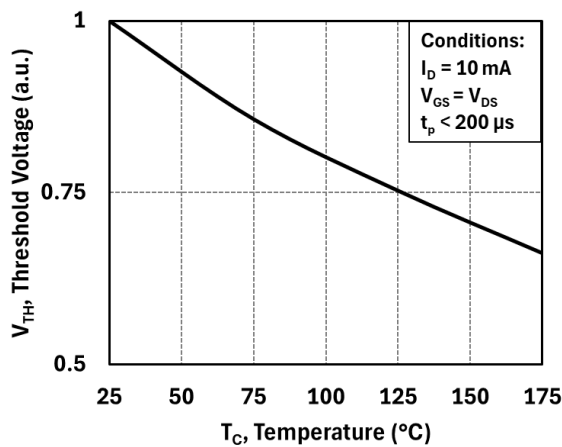


Figure 9: Threshold Voltage vs. Temperature

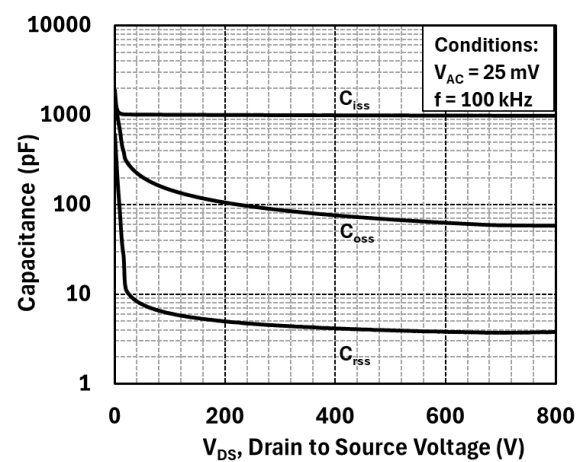


Figure 10: Capacitances vs. Drain-Source Voltage (0-1000 V)

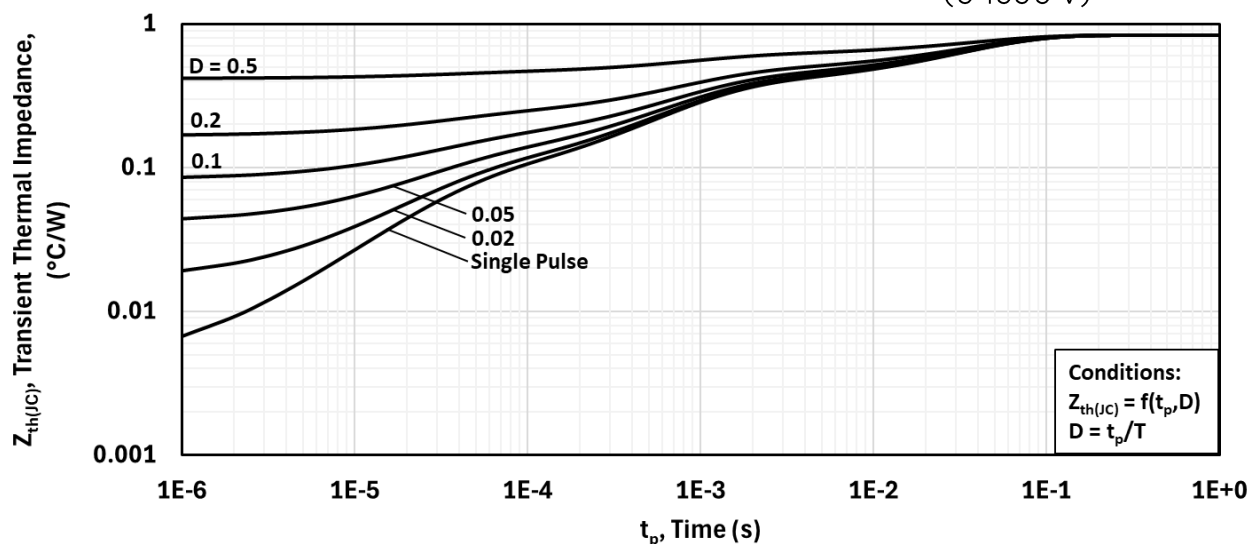


Figure 11: Transient Thermal Impedance





Typical Performance

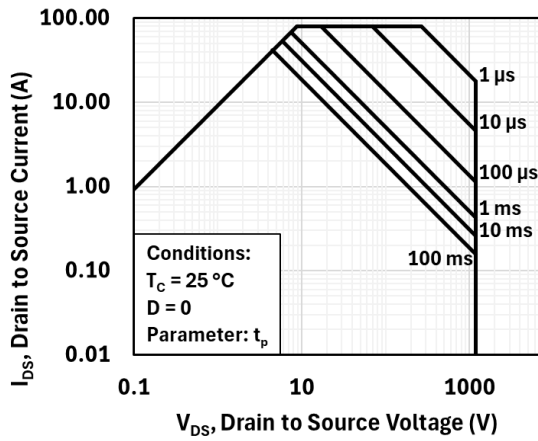


Figure 12: Safe Operating Area

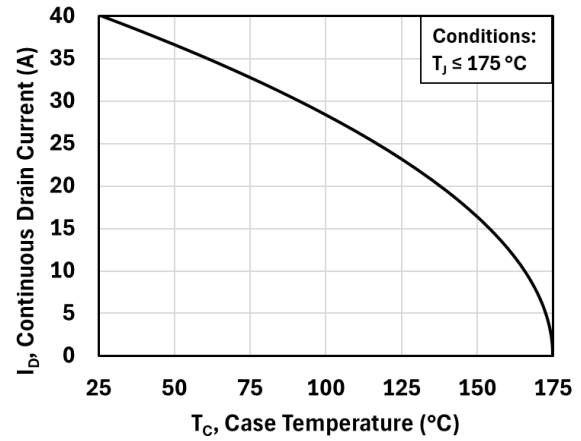


Figure 13: Current De-rating Curve

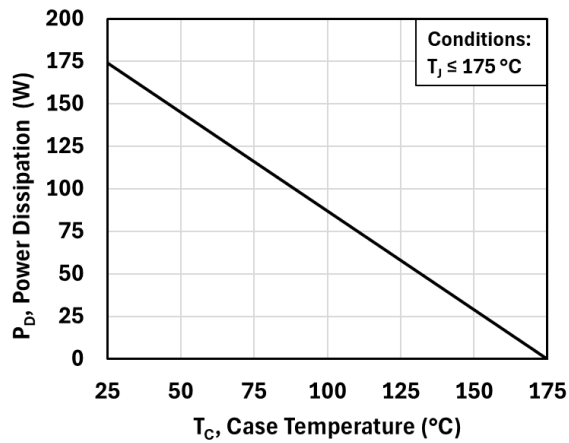


Figure 14: Power De-rating Curve

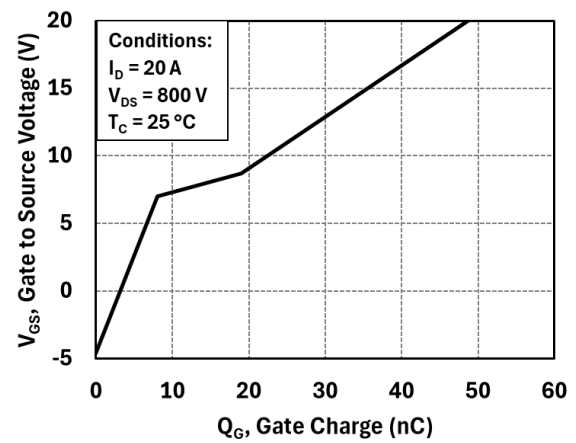


Figure 15: Gate Charge Characteristics

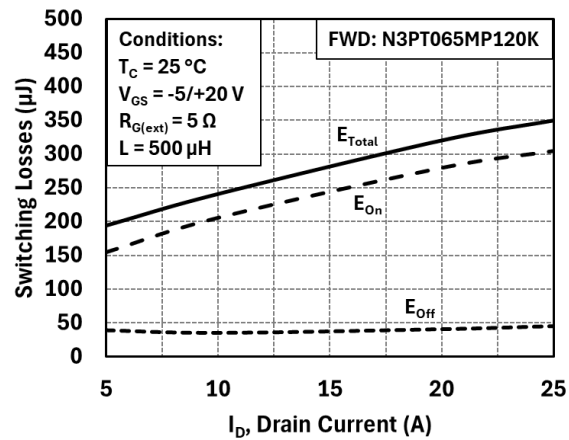


Figure 16: Inductive Switching Energy vs. Drain Current ($V_{DD} = 800\text{ V}$)

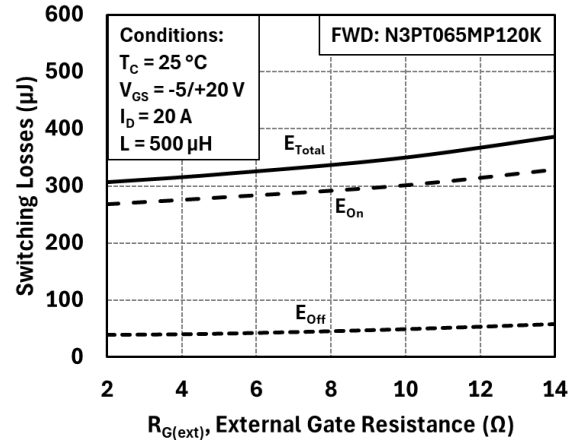


Figure 17: Inductive Switching Energy vs. $R_{G(ext)}$ ($V_{DD} = 800\text{ V}$)





Typical Performance

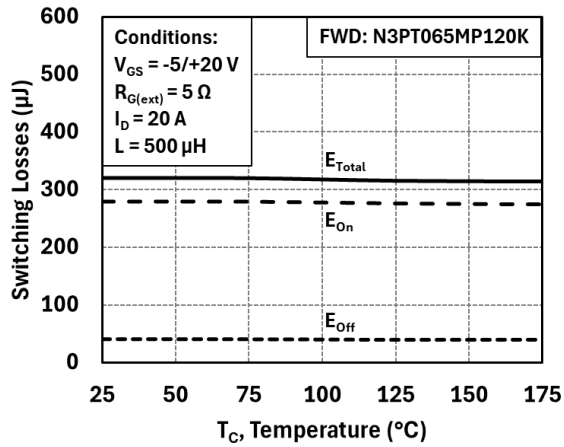


Figure 18: Inductive Switching Energy vs. Temperature ($V_{DD} = 800$ V)

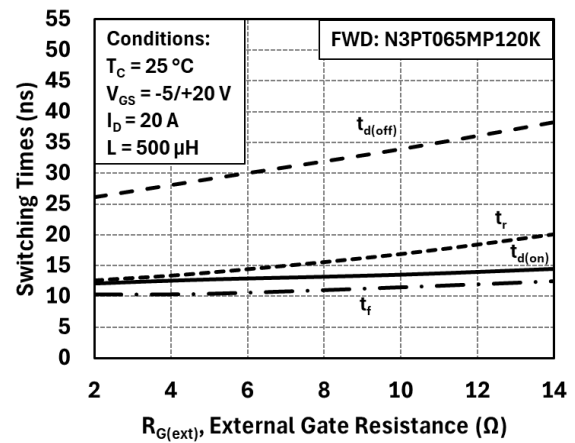


Figure 19: Switching Times vs. $R_{G(ext)}$ ($V_{DD} = 800$ V)

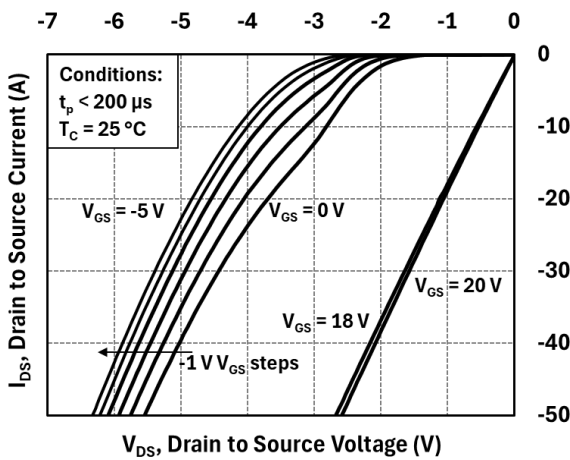


Figure 20: Body Diode Characteristics at 25 °C

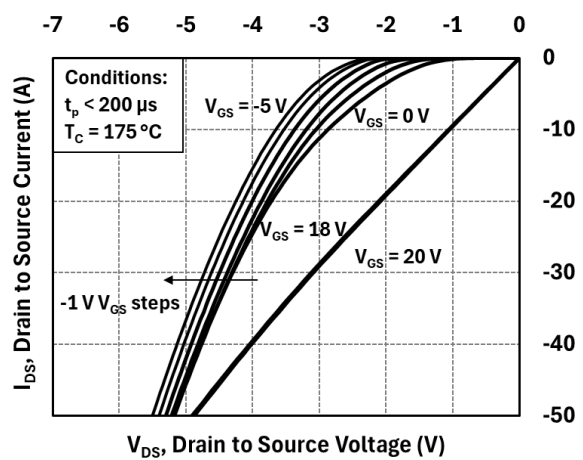


Figure 21: Body Diode Characteristics at 175 °C

Dynamic Testing Circuit Schematics

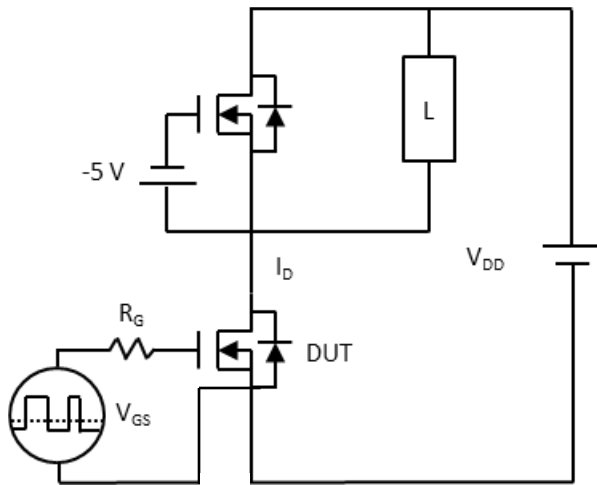


Figure 22: Inductive Load Switching Test Circuit

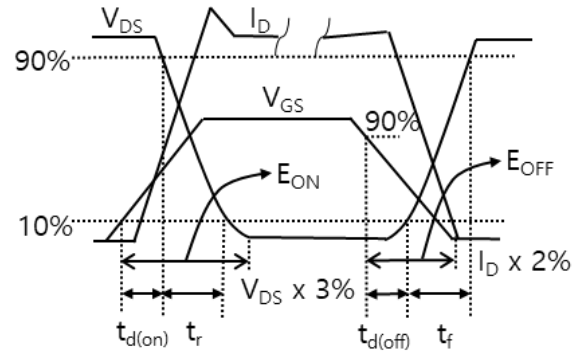


Figure 23: Inductive Load Switching Test Waveforms

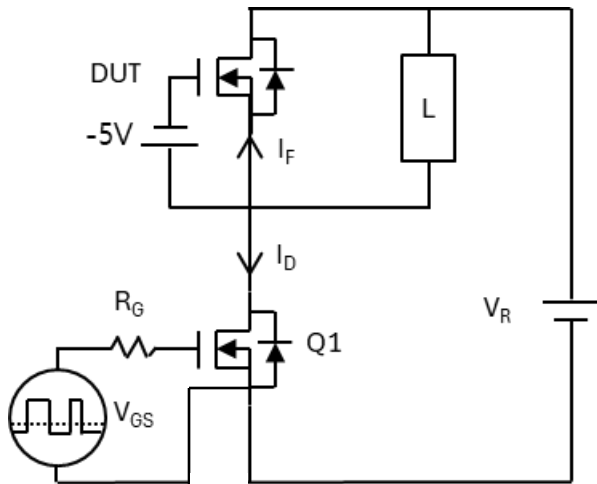


Figure 24: Reverse Recovery Test Circuit

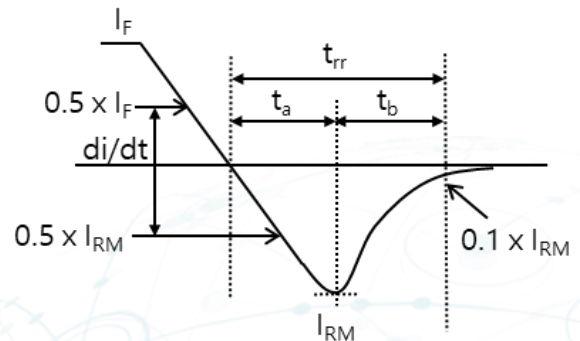


Figure 25: Body Diode Reverse Recovery Test Waveforms

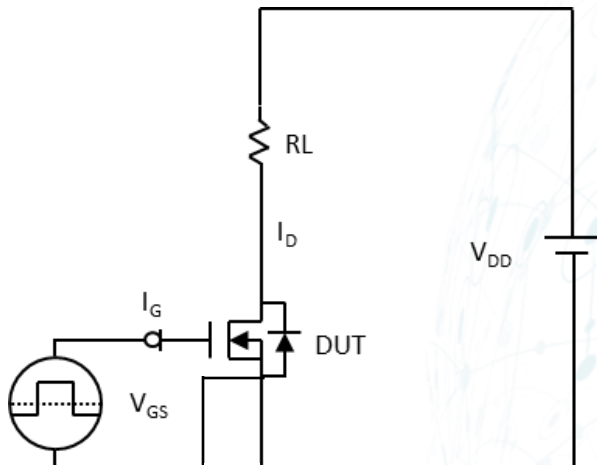


Figure 26: Gate Charge Test Circuit

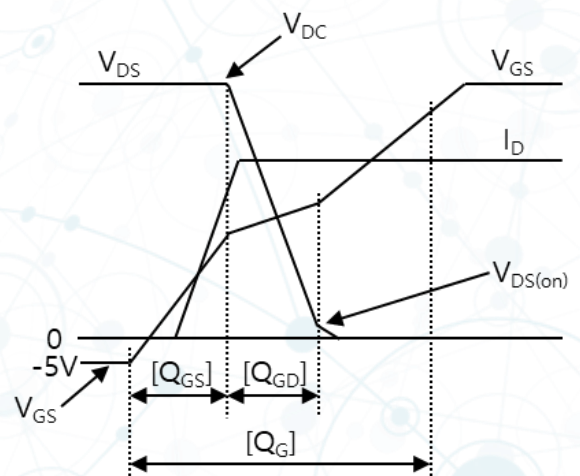
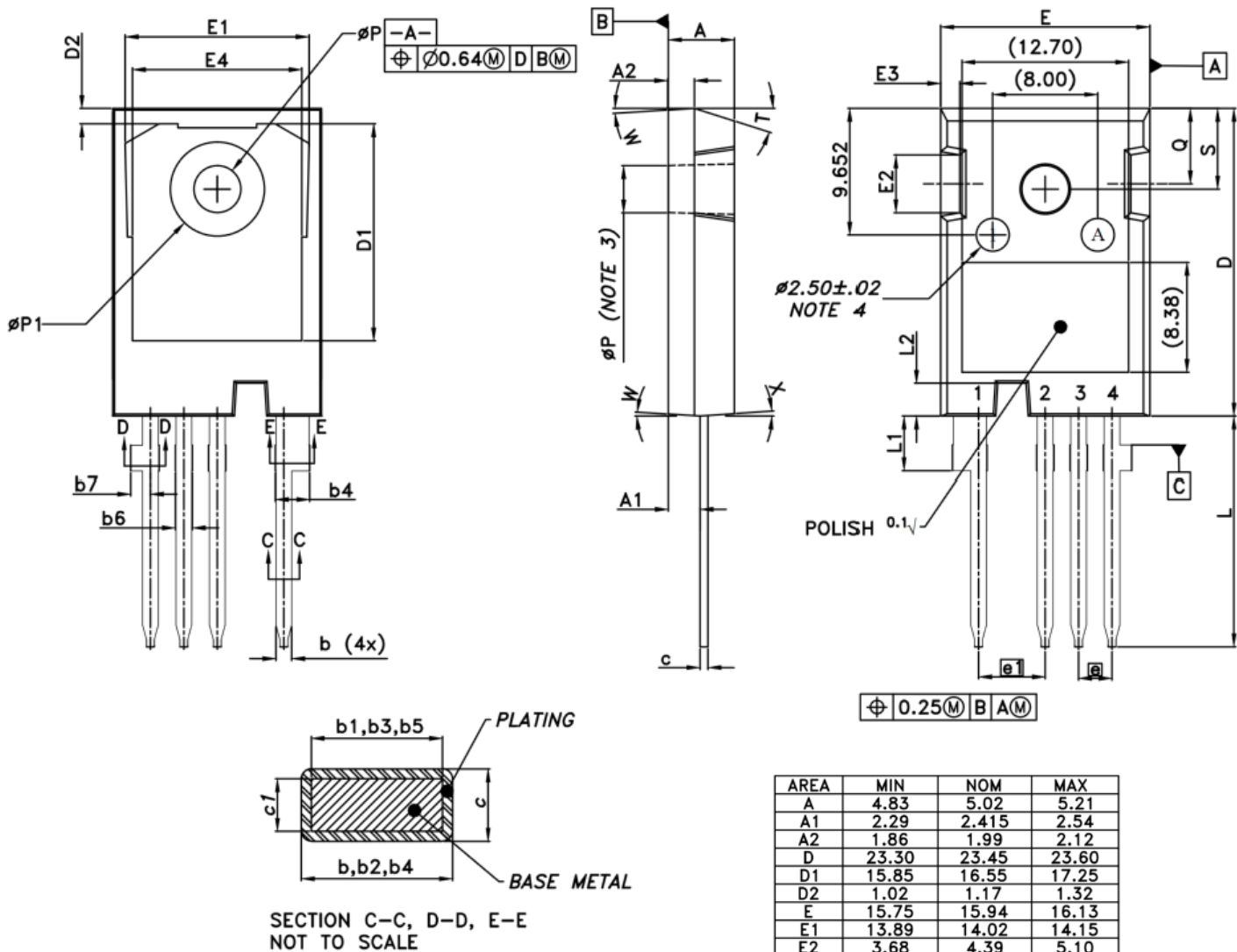


Figure 27: Gate Charge Test Waveforms



Package Dimensions



NOTES:

1. DIMENSIONS ARE IN MILLIMETERS
2. DIMENSION D & E DO NOT INCLUDE MOLD FLASH, MOLD FLASH SHALL NOT EXCEED 0.127 MM PER SIDE. THESE DIMENSIONS ARE MEASURED AT THE OUTERMOST EXTREME OF THE PLASTIC BODY.
3. ϕP TO HAVE A MAXIMUM DRAFT ANGLE OF 1.5° TO THE TOP OF THE PART WITH A MAXIMUM HOLE DIAMETER OF 3.65mm.
4. EJECTION MARK DEPTH 0.10^{+0.15}_{-0.08}

AREA	MIN	NOM	MAX
A	4.83	5.02	5.21
A1	2.29	2.415	2.54
A2	1.86	1.99	2.12
D	23.30	23.45	23.60
D1	15.85	16.55	17.25
D2	1.02	1.17	1.32
E	15.75	15.94	16.13
E1	13.89	14.02	14.15
E2	3.68	4.39	5.10
E3	1.00	1.45	1.90
E4	12.38	12.91	13.43
e	2.540 BSC		
e1	5.080 BSC		
L	17.31	17.57	17.82
L1	3.97	4.17	4.37
L2	2.35	2.50	2.65
b	1.07	-	1.33
b1	1.07	1.20	1.28
b2	2.39	-	2.64
b3	2.39	-	2.69
b4	2.39	-	2.94
b5	2.39	2.53	2.84
b6	1.07	-	1.60
b7	1.30	-	1.70
c	0.55	-	0.68
c1	0.55	0.60	0.65
ϕP	3.51	3.58	3.65
Q	5.49	5.75	6.00
S	6.04	6.15	6.30
$\phi P1$	7.18 REF		
T	17.5° REF		
W	3.5° REF		
X	4° REF		



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