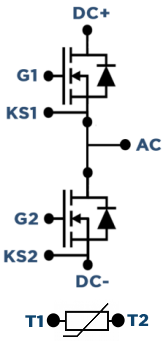
NH3T008MP120F2

1200 V 8 mΩ Silicon Carbide Half-Bridge Power Module

V_{DS}	I_D	$R_{DS(on)}$	Configuration
1200 V	200 A	8 mΩ	Half-Bridge



Features

- State-of-the-art SiC MOSFET technology
- Reliable gate oxide process
- 100% avalanche tested
- Press-fit package for design flexibility
- Baseplate-less for low thermal resistance

Benefits

- Higher system efficiency
- Reduced cooling requirements
- Increased power density
- Increased system switching frequency
- Enhanced system reliability
- Reduced total harmonic distortion

Applications

- Motor drives
- Solar PV inverters
- EV onboard chargers
- Server power supplies
- Energy storage systems
- EV fast charging stations
- Solid-state power controllers
- Uninterruptible power supplies

Maximum Ratings

Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit	Note
Drain-Source Voltage	$V_{(BR)DSS}$	T_C = 25 °C	1200	-	-	V	
Gate-Source Voltage	$V_{GS(max)}$		-10	-	25	V	
	$V_{GS,op}$	Recommended Operation	-	-5/+20	-		
Continuous Drain Current	I_D	V_{GS} = 20 V, T_C = 25 °C	-	-	200	A	Fig. 18
		V_{GS} = 20 V, T_C = 100 °C	-	-	200		
Pulsed Drain Current	$I_{D(pulse)}$	T_C = 25 °C t_P limited by $T_{j(max)}$	-	-	400	A	Fig. 16
Operating Temperature	T_J		-55	-	175	°C	

Thermal and Package Characteristics

Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit	Note
Case Isolation Voltage	V_{Iso}	RMS, f = 60 Hz, t = 1 minute	-	3.5	4.5	kV	
Stray Inductance	L_{Stray}	Between DC+ and DC-, f = 10 MHz	-	9.3	-	nH	
Case Temperature	T_C		-	-	150	°C	
Weight	W_T		-	39	-	g	
Mounting Torque	T_M	M4 bolts	-	2	2.3	Nm	
Comparative Tracking Index	CTI		-	600	-		
Clearance (Terminal to Terminal)	$d_{Cl(TT)}$			6		mm	
Clearance (Terminal to Heatsink)	$d_{Cl(TH)}$			14		mm	
Creepage (Terminal to Terminal)	$d_{Cr(TT)}$			8		mm	
Creepage (Terminal to Heatsink)	$d_{Cr(TH)}$			15.5		mm	

Electrical Characteristics (T_J = 25 °C unless otherwise specified)

MOSFET STATIC CHARACTERISTICS (Per Position)

Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit	Note
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS} = 0 V, I_D = 100 µA	1200	-	-	V	
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 1200 V, V_{GS} = 0 V	-	1	100	µA	
Gate Threshold Voltage	$V_{GS(th)}$	V_{GS} = V_{DS}, I_D = 100 mA	1.8	2.6	4	V	
Gate-Source Leakage Current	I_{GSS}	V_{GS} = -10 / +25 V, V_{DS} = 0 V	-	-	±100	nA	
Transconductance	g_{fs}	V_{DS} = 20 V, I_D = 100 A	-	59.1	-	S	Fig. 8
Drain-Source On-State Resistance	$R_{DS(on)}$	V_{GS} = 20 V, I_D = 100 A	-	6.7	10	mΩ	Fig. 4 Fig. 5 Fig. 6
		V_{GS} = 20 V, I_D = 100 A, T_J = 175 °C	-	9.5	-		
		V_{GS} = 18 V, I_D = 100 A	-	7.5	-		
		V_{GS} = 18 V, I_D = 100 A, T_J = 175 °C	-	10.6	-		

DYNAMIC CHARACTERISTICS

Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit	Note
Input Capacitance	C_{iss}	V_{GS} = 0 V, V_{DS} = 600 V, V_{AC} = 25 mV, f = 100 kHz	-	8784	-	pF	Fig. 10
Output Capacitance	C_{oss}		-	728	-		
Reverse Capacitance	C_{rss}		-	109	-		
Gate-Source Charge	Q_{GS}	V_{DS} = 600 V, V_{GS} = -5 / +20 V, I_D = 50 A	-	67	-	nC	Fig. 11
Gate-Drain Charge	Q_{GD}		-	103	-		
Total Gate Charge	Q_G		-	530	-		
Internal Gate Resistance	$R_{G(int)}$	V_{DS} = 0 V, f = 1 MHz	-	0.5	-	Ω	
Turn-On Switching Energy	E_{ON}	V_{DD} = 600 V, I_D = 100 A, V_{GS} = -5 / +20 V, $R_{G(ext)}$ = 5 Ω, L = 110 µH	-	1887	-	µJ	Fig. 12 Fig. 13
Turn-Off Switching Energy	E_{OFF}		-	1631	-		
Total Switching Energy	E_{TOT}		-	3518	-		
Turn-On Delay Time	$t_{d(on)}$	V_{DD} = 600 V, I_D = 100 A, V_{GS} = -5 / +20 V, $R_{G(ext)}$ = 5 Ω, L = 110 µH Timing relative to V_{DS} Inductive Load	-	38	-	ns	Fig. 14 Fig. 15
Rise Time	t_r		-	46	-		
Turn-Off Delay Time	$t_{d(off)}$		-	112	-		
Fall Time	t_f		-	29	-		
Thermal Resistance, Junction to Case	$R_{th(JC)}$	Per MOSFET		0.27	-	°C/W	

BODY DIODE CHARACTERISTICS

Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit	Note
Diode Forward Voltage	V_{SD}	V_{GS} = -5 V, I_{SD} = 100 A	-	4.18	-	V	Fig. 20
		V_{GS} = -5 V, I_{SD} = 100 A, T_C = 175 °C	-	3.89	-	V	Fig. 21
Continuous Diode Forward Current	I_S	V_{GS} = -5 V	-	148	-	A	
Reverse Recovery Time	t_{rr}	V_R= 600 V, I_{SD} = 100 A, V_{GS} = -5 V, di_F/dt = 6000 A/µs	-	31	-	ns	
Reverse Recovery Charge	Q_{rr}		-	1314	-	nC	
Peak Reverse Recovery Current	I_{RRM}		-	68.9	-	A	

Typical Performance

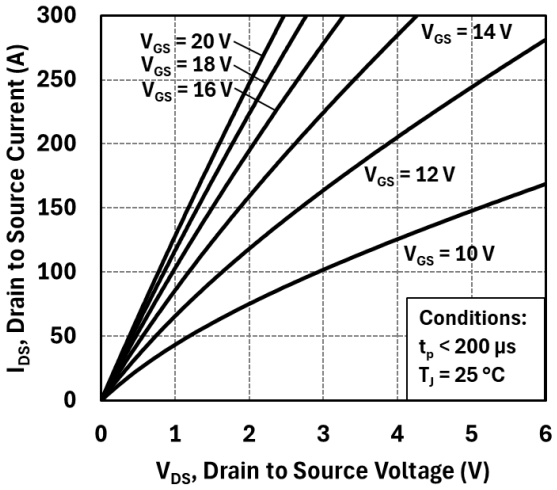


Figure 1: Output Characteristics at 25 °C

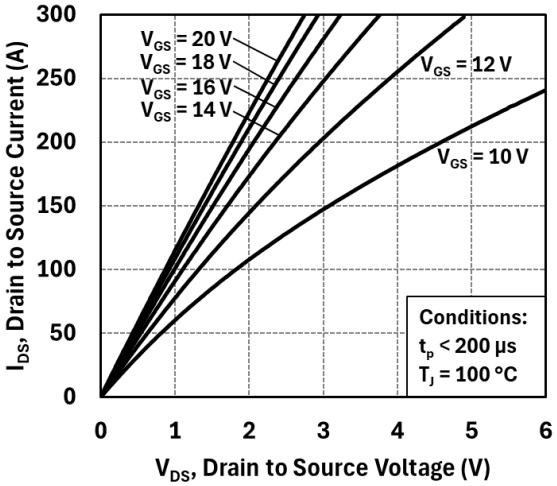


Figure 2: Output Characteristics at 100 °C

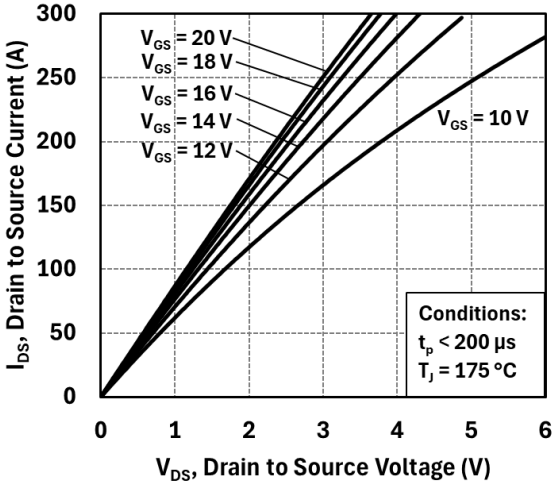


Figure 3: Output Characteristics at 175 °C

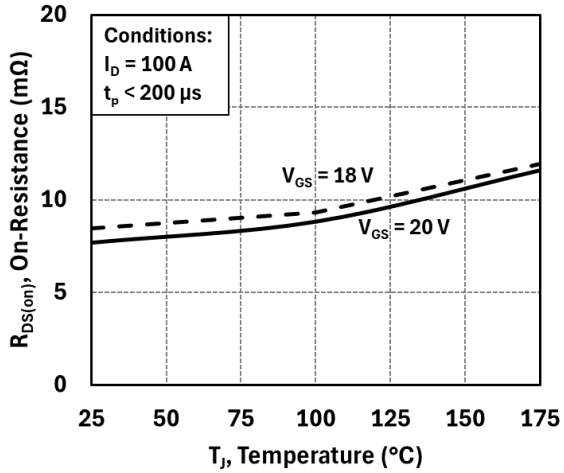


Figure 4: On-Resistance vs. Temperature

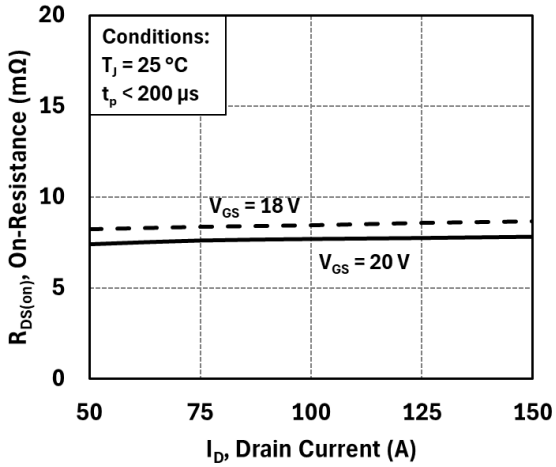


Figure 5: On-Resistance vs. Drain Current

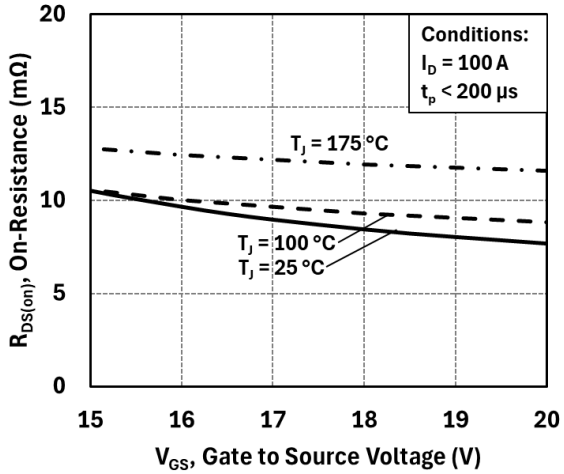


Figure 6: On-Resistance vs. Gate Voltage

Typical Performance

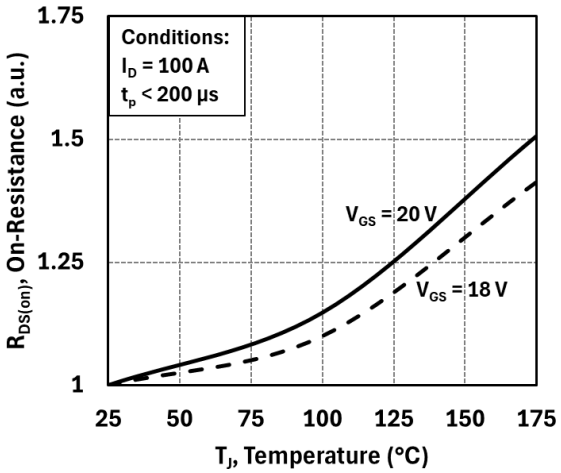


Figure 7: Normalized On-Resistance vs. Temperature

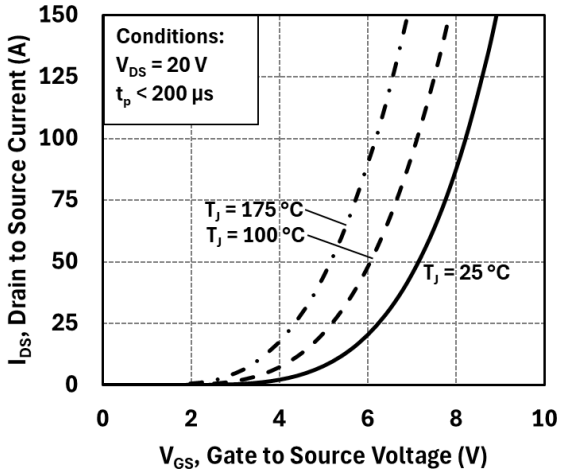


Figure 8: Transfer Characteristics

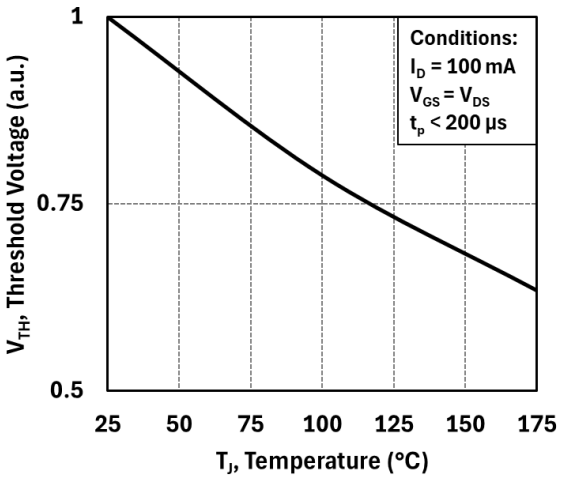


Figure 9: Threshold Voltage vs. Temperature

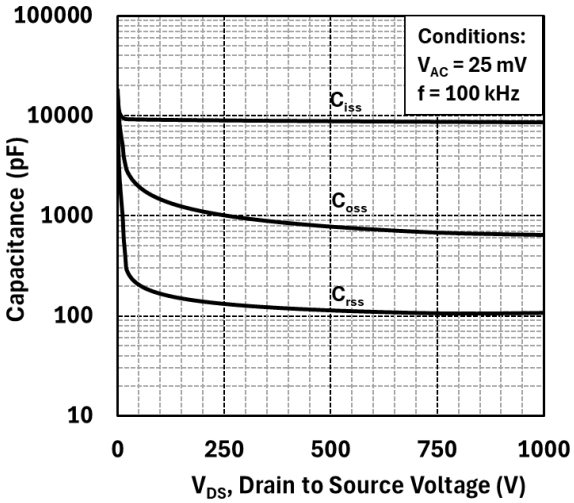


Figure 10: Capacitances vs. Drain-Source Voltage (0-1000 V)

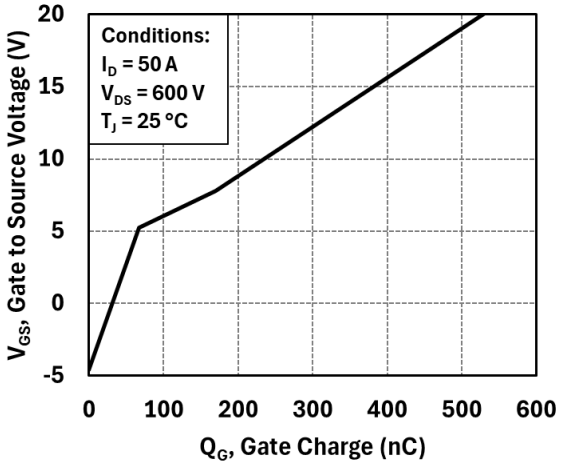


Figure 11: Gate Charge Characteristics

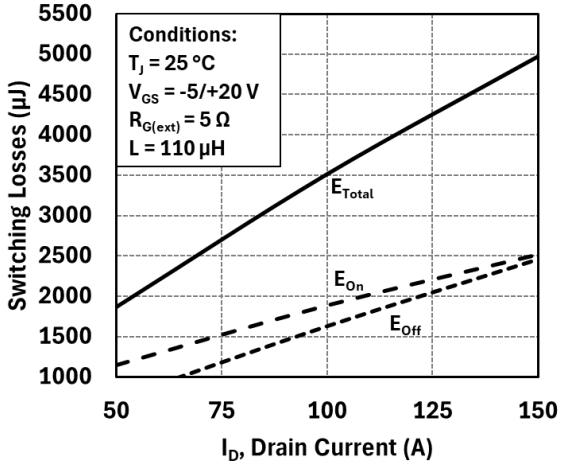


Figure 12: Inductive Switching Energy vs. Drain Current (V_{DD} = 600 V)

Typical Performance

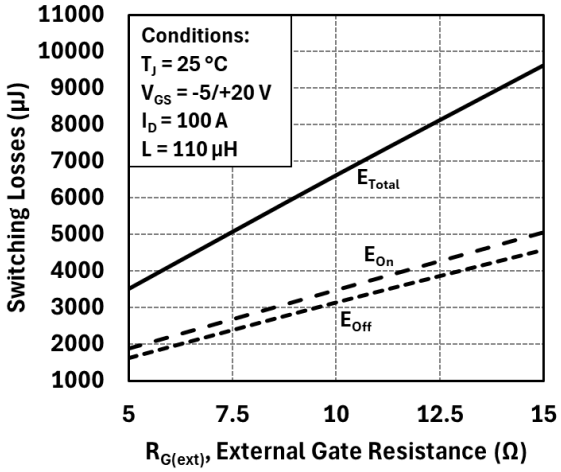


Figure 13: Inductive Switching Energy vs. $R_{G(ext)}$ (V_{DD} = 600 V)

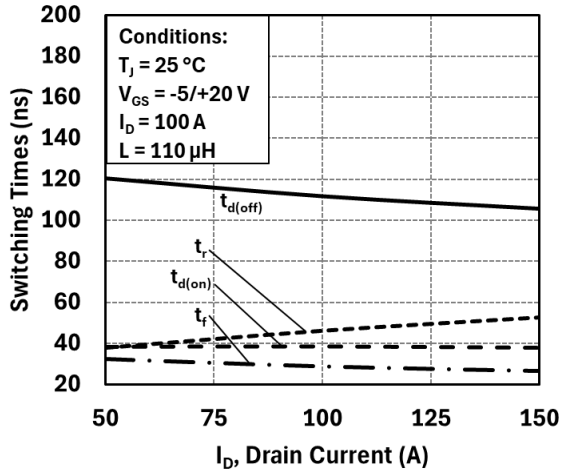


Figure 14: Switching Times vs. Drain Current (V_{DD} = 600 V)

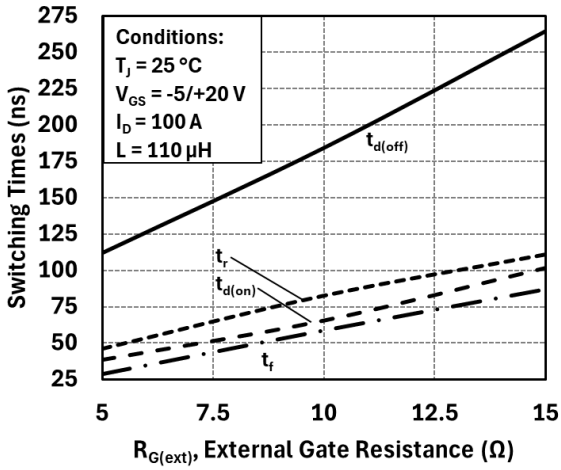


Figure 15: Switching Times vs. $R_{G(ext)}$ (V_{DD} = 600 V)

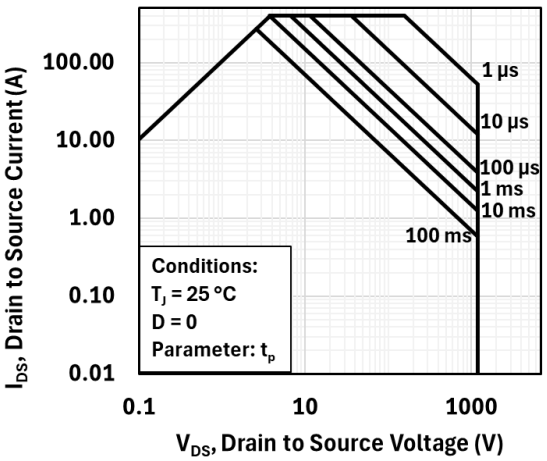


Figure 16: Forward Bias Safe-Operating-Area

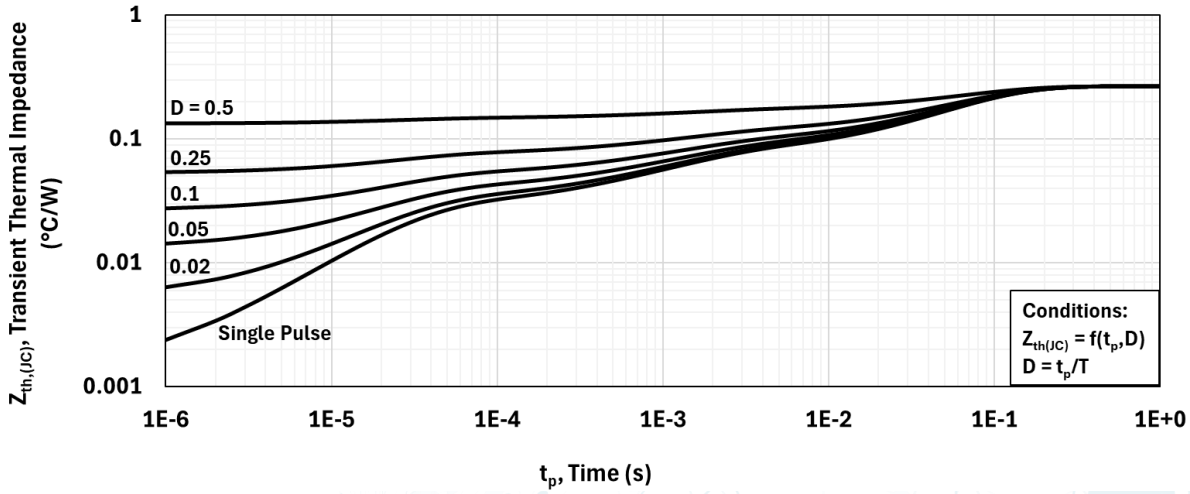


Figure 17: Transient Thermal Impedance

Typical Performance

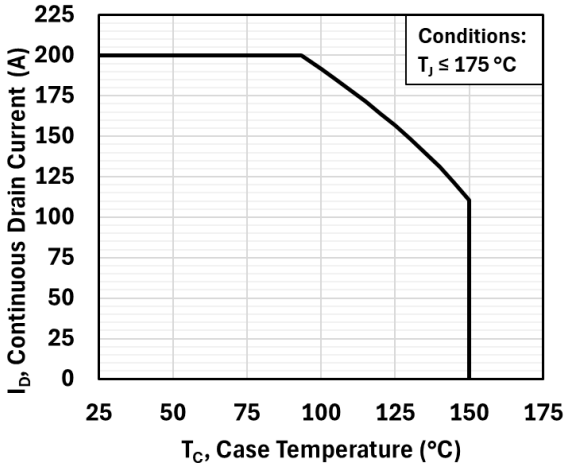


Figure 18: Current De-Rating vs. Temperature

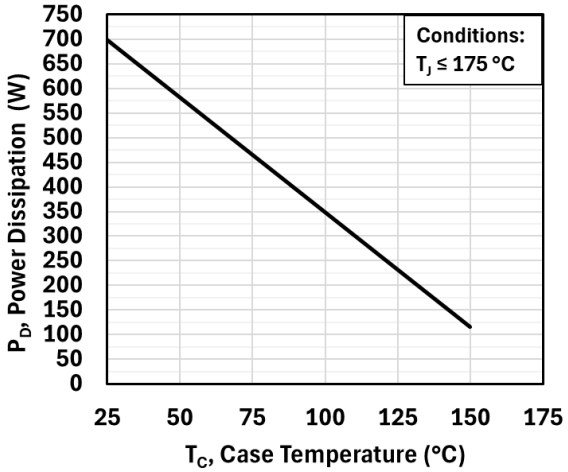


Figure 19: Power De-Rating vs. Temperature

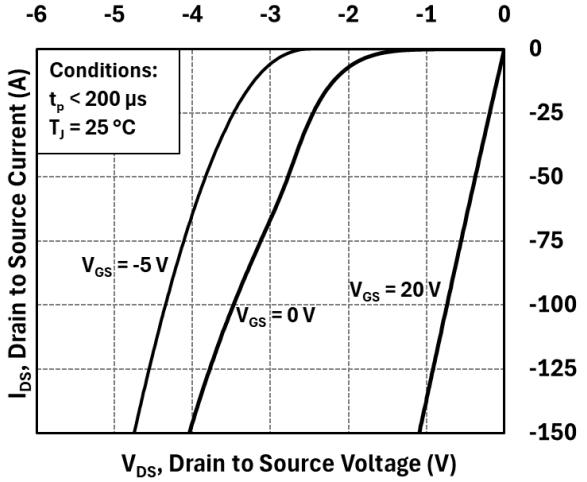


Figure 20: Body Diode Characteristics at 25 °C

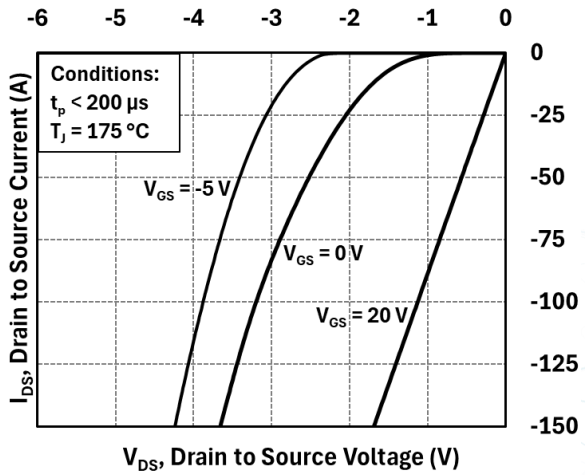


Figure 21: Body Diode Characteristics at 175 °C

NTC Thermistor Characterization

Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit	Note
Rated Resistance	R_{NTC}	25±0.05 °C	4.75	5.0	5.25	kΩ	Fig. 22
Beta Value	$\beta_{25/50}$	25±0.05 °C, 50±0.05 °C	3312	3380	3448	K	
Time Constant	τ	In still air	-	≤10	-	S	
Dissipation Factor	δ	In still air	-	≥2.4	-	mW /°C	
Power Dissipation	P_{Max}	Ambient temperature+25°C	-	80	-	mW	

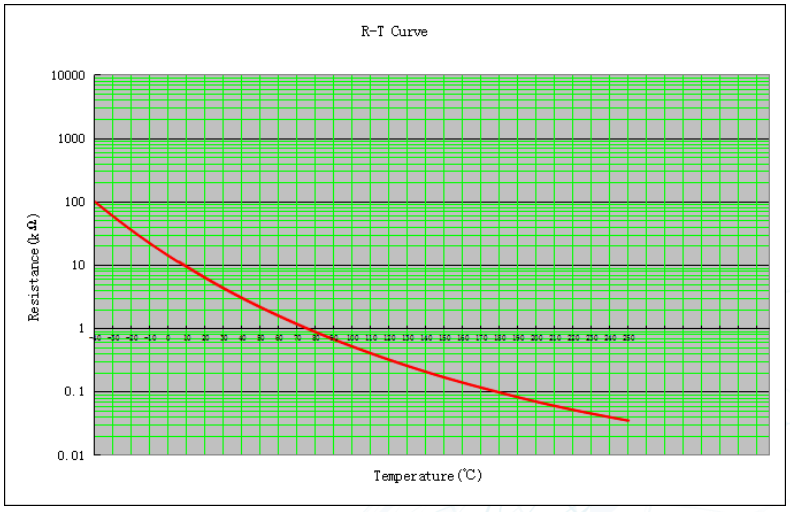
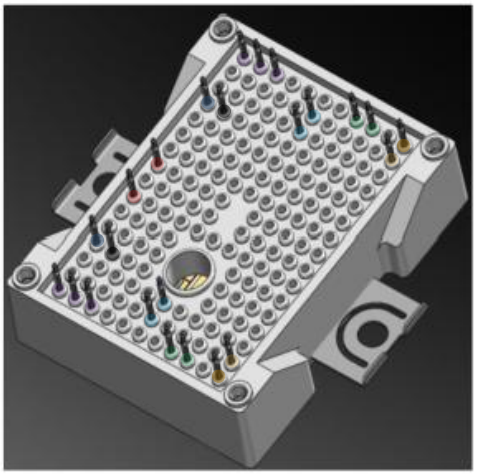
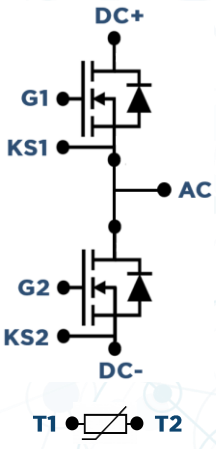


Figure 22: Nominal NTC Resistance vs. NTC Temperature

Pinout

DC+
DC-
AC
Gate 1
Source 1
Gate 2
Source 2
NTC Terminals





Dynamic Testing Circuit Schematics

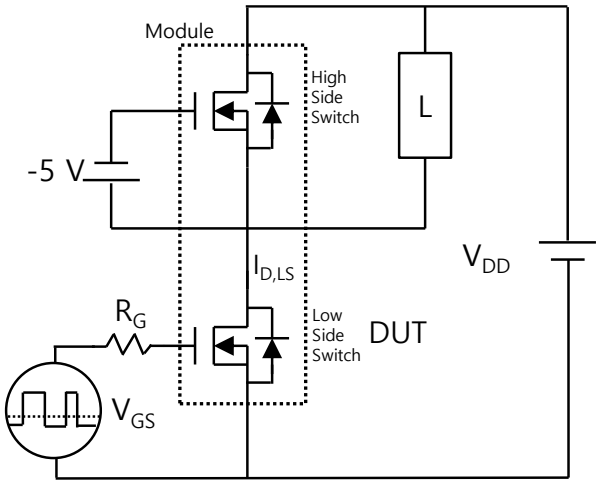


Figure 23: Inductive Load Switching Test Circuit

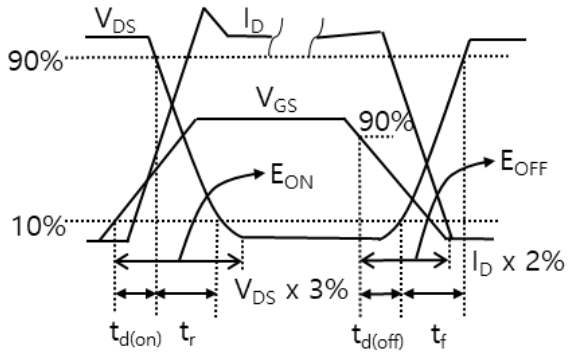


Figure 24: Inductive Load Switching Test Waveforms

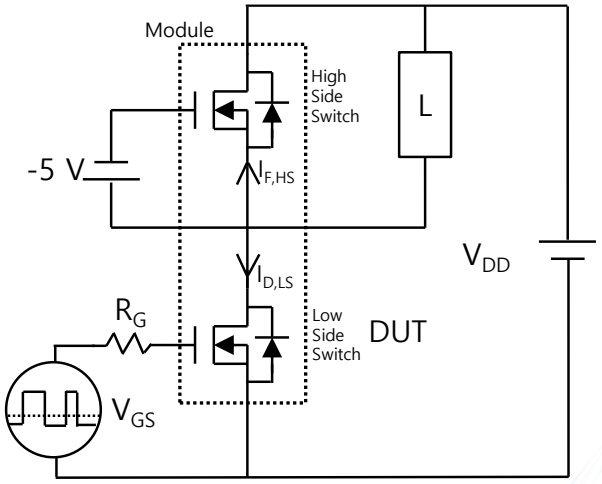


Figure 25: Reverse Recovery Test Circuit

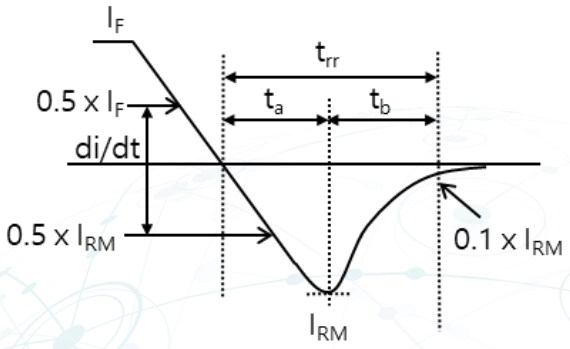


Figure 26: Body Diode Reverse Recovery Test Waveforms

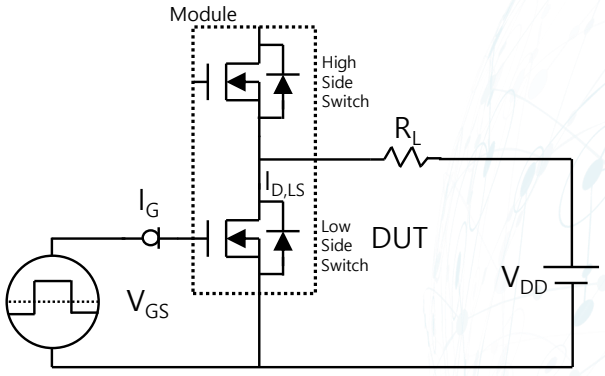


Figure 27: Gate Charge Test Circuit

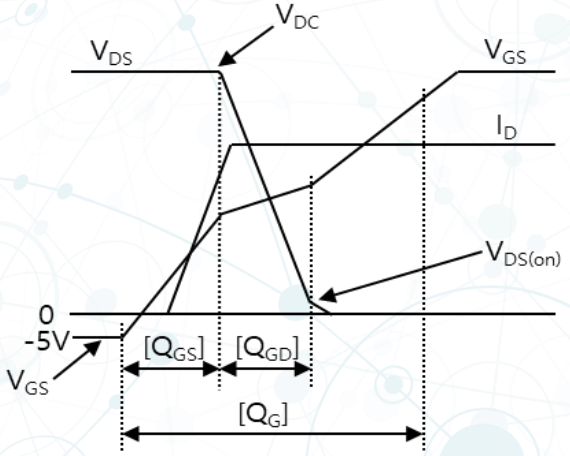
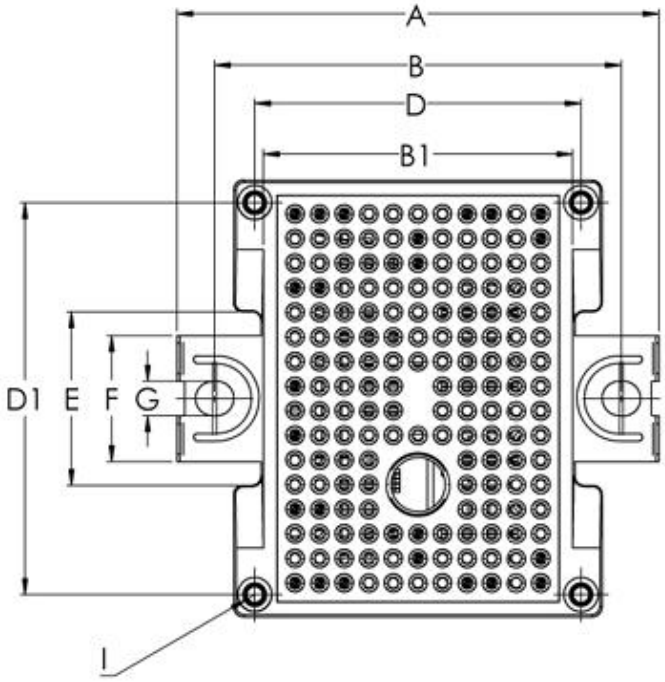
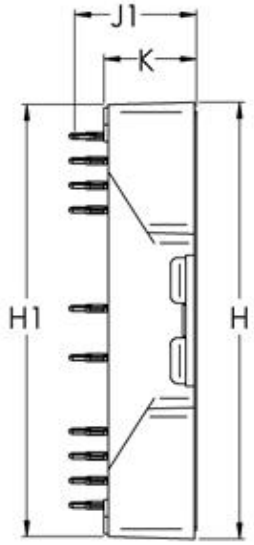
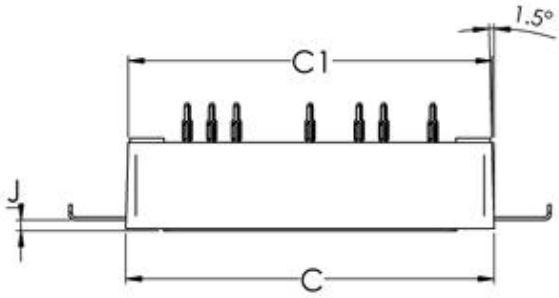


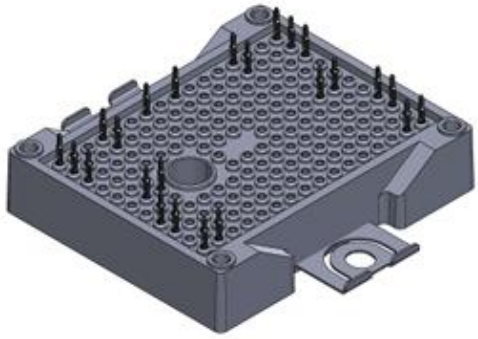
Figure 28: Gate Charge Test Waveforms

Package Dimensions









AREA	MIN	NOM	MAX
A	62.30	62.80	63.30
B	52.80	53.00	53.40
B1	40.70	40.90	41.30
C	47.70	48.00	48.30
C1	47.11	47.41	47.71
D	42.30	42.50	42.70
D1	50.80	51.00	51.20
E	22.40	22.70	23.00
F	16.20	16.40	16.60
G	4.40	4.50	4.60
H	56.40	56.80	57.00
H1	55.81	56.21	56.41
I	⌀2.20	⌀ 2.30	⌀2.40
J	1.075	1.40	1.70
J1	15.90	16.40	16.90
K	11.70	12.05	12.40

Note:

- Signal Pin hole - grid 3.2mm
- Tolerance of hole pattern ⌖ 0.1
- Signal Pin drill diameter 1.30mm
- Rib matrix thickness 0.9 ±0.2mm
- Brace thickness 0.4mm

Material:
1. Plastic Case PBT+30%GF (D202G30 White)
2. Cosmetic Treatment - Polish (#1000 - #2000)

Warranty & Disclaimers

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